

# Chapter 12

## Algorithmic State Machine

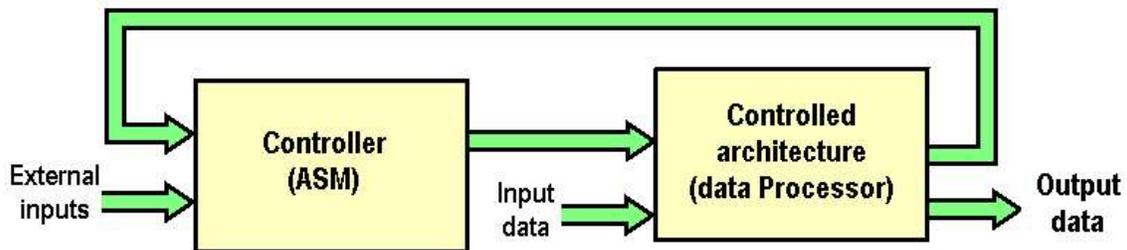
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### 12.0 Introduction

In Chapter 10, we introduced two models of synchronous sequential network, which are Mealy and Moore machines. In this chapter, we would like to introduce another approach of designing synchronous sequential network using flowchart, which is similar to those used in computer programming. This is called *algorithmic state machine* ASM. Designing using ASM allows handling of more complex system than state diagram shown in earlier chapter.

### 12.1 Algorithmic State Machine

An approach of digital design is to partition the system into a controller and a controlled architecture also called data processor, which is shown in Fig. 12.1.



**Figure 12.1:** Partition of digital system

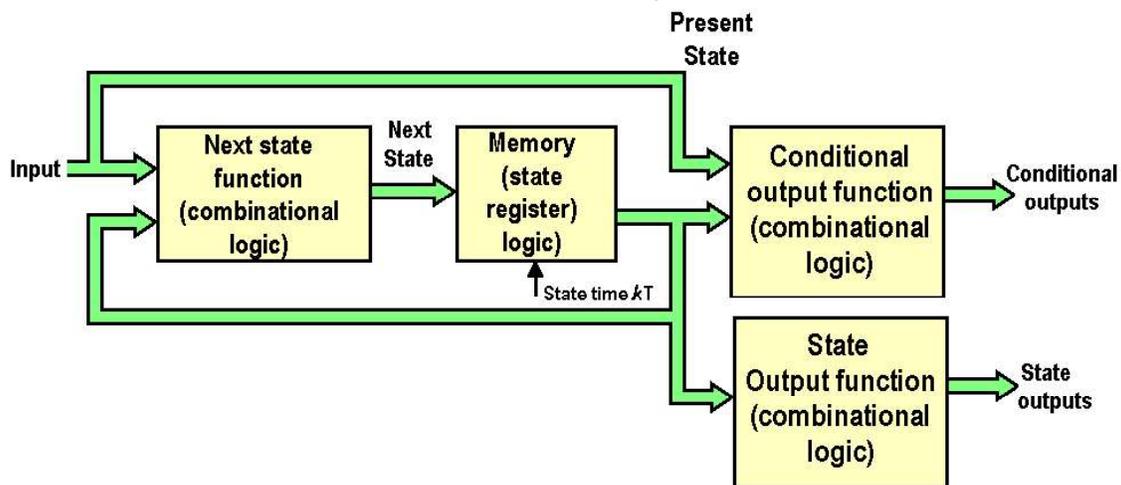
Data processor is a hardware required for data manipulation that may consist of adder, subtractor, shift register, and etc and output the results. In addition to this function, the data processor also provides status of the data manipulation to the controller.

The controller, which is also termed as ASM, provides sequence of command to data processor. It is called *ASM* because it consists of well defined finite number of step to the solution of a process.

The external input is used to provide the task required to be carried out by the controller. The input data is used in the manipulation.

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The model of algorithmic state machine ASM is shown in Fig. 12.2. The machine is viewed as the combination of Mealy and Moore machines.

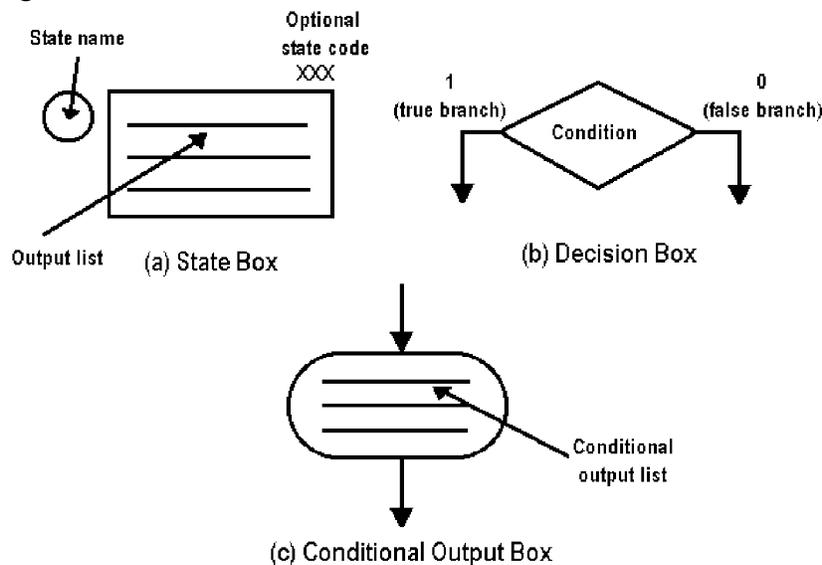


**Figure 12.2:** Model of Algorithmic State Machine

Next state and memory blocks are similar for both Mealy and Moore machines. Conditional output function block is similar to that of a Mealy machine, whilst state output function block is similar to that of a Moore machine.

## 12.2 Algorithmic State Machine Chart

The algorithmic state machine SM chart can be divided into three blocks namely the state box, the decision box, and the conditional output box. They are shown in Fig. 12.3.

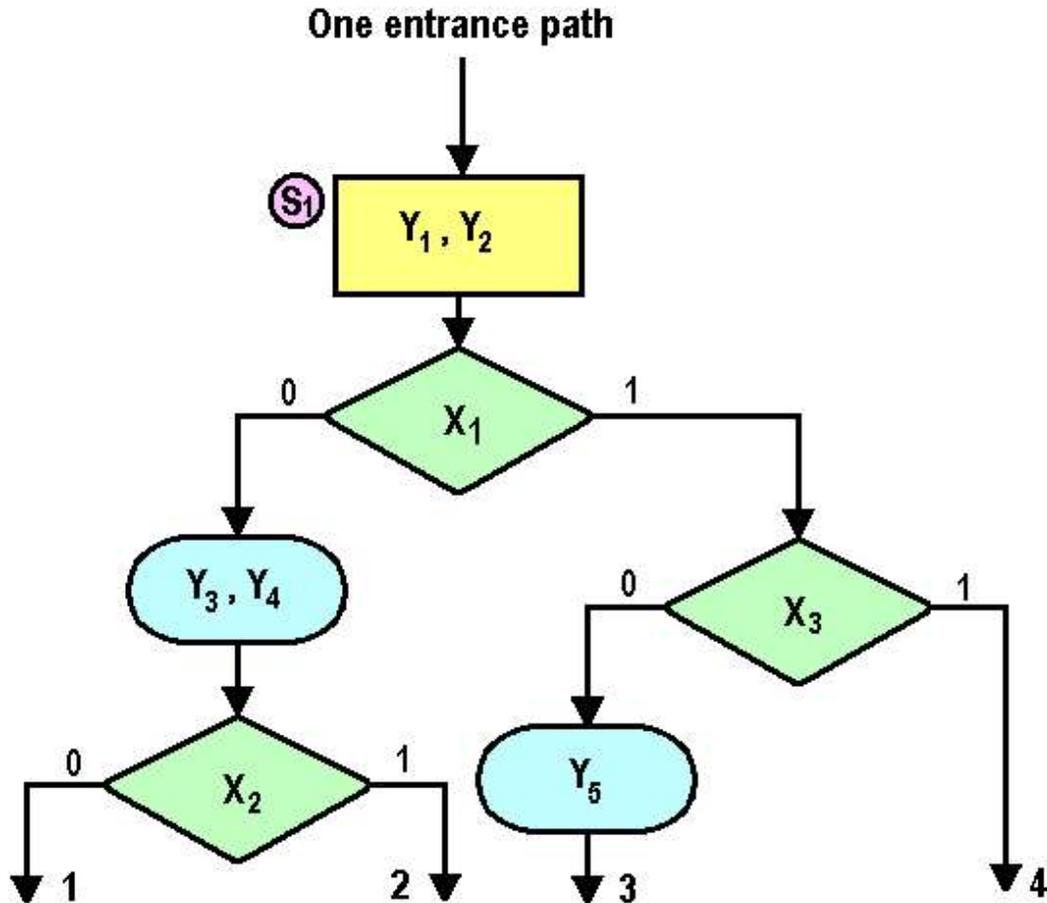


**Figure 12.3:** The algorithmic state machine blocks

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The state box contains an output list, state name, and optional state code. The decision box is a usual diamond shaped symbol with true and false evaluate to decide the branches. The conditional output box contains conditional output list. The conditional outputs depend on both the state of system and the inputs.

Let's consider an ASM chart shown in Fig. 12.4 and use it to explain the flow of the sequence.



**Figure 12.4:** An ASM chart showing the state box, conditional box, and decision box

When state  $S_1$  entered, output  $Y_1$  and  $Y_2$  become “1”. If inputs  $X_1$  and  $X_2$  are both equal to 0,  $Y_3$  and  $Y_4$  are also “1”, and at the end of state time the machine goes to the next state via exit path 1. If inputs  $X_1 = “0”$  and  $X_2 = “1”$ ,  $Y_3$  and  $Y_4$  are “1”, the exit to next state is via path 2.

On the other hand, if  $X_1 = “1”$  and  $X_3 = “0”$ , the output  $Y_5$  is “1” and exit to the next state will occur via exit path 3. If  $X_1 = “1”$  and  $X_3 = “1”$ , the exit to the next state will occur via path 4.

### 12.3 Conversion of State Diagram to Algorithmic State Machine Chart

Let's consider the state diagram of a SR flip-flop and see how it is being converted into an ASM chart. From the excitation equation of an SR flip-flop, which is  $Q_{n+1} = S + Q_n \cdot \bar{R}$ , the state diagram of a SR flip-flop is derived and shown in Fig. 12.5.

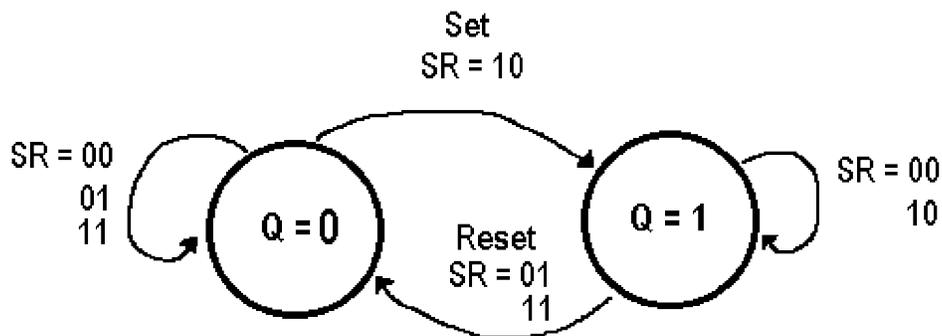


Figure 12.5: State diagram of a SR flip-flop

The simplified form with Boolean expressions is shown in Fig. 12.6.

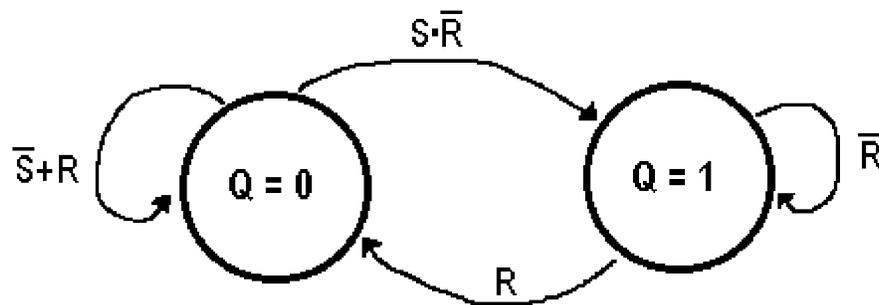


Figure 12.6: The simplified form of state diagram for SR flip-flop

Based on the state diagram shown in Fig. 12.5, the ASM chart of the SR flip-flop is shown in Fig. 12.7.

The initial state of the flip-flop is  $Q = "0"$ , when the decision  $S \cdot \bar{R}$  is true, the flip-flop will change state to  $Q = "1"$ . When it is not true, which shall mean  $\overline{S \cdot \bar{R}} = S + R$ , it would hold its state at  $Q = "0"$ .

When the decision  $\bar{R}$  is true, the flip-flop will hold its state at  $Q = "1"$ . When the decision  $\bar{R}$  is not true, which is  $R$  is true, the flip-flop will change state to  $Q = "0"$ .

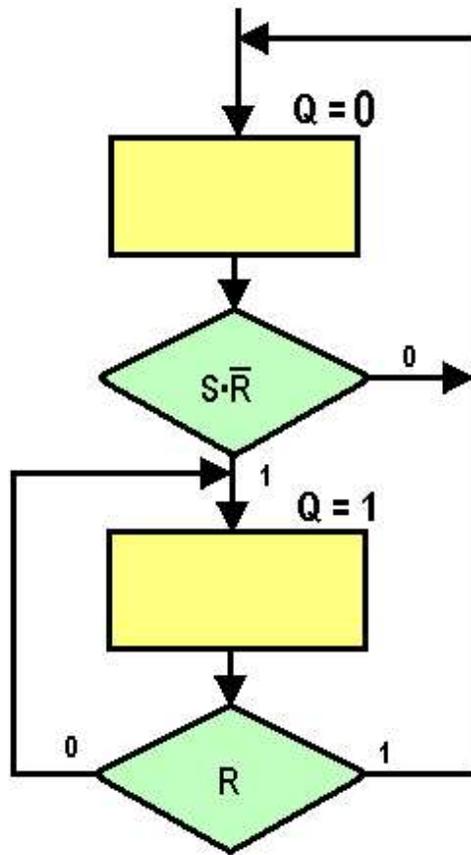


Figure 12.7: The ASM chart of SR flip-flop

Let's consider an example of sequential network shown in Fig. 12.8. This sequential network contains both Mealy and Moore outputs. The Mealy output is depending on the present state and input state X. Thus, output  $Y_1$  and  $Y_2$  should be conditional outputs and they are to be resided in the conditional box. Output  $Y_a$ ,  $Y_b$ , and  $Y_c$  are Moore outputs. They do not depend on the state of input X. Thus they should reside in the state box. Input X can be either "0" or "1". Thus, it should be resided in decision box.

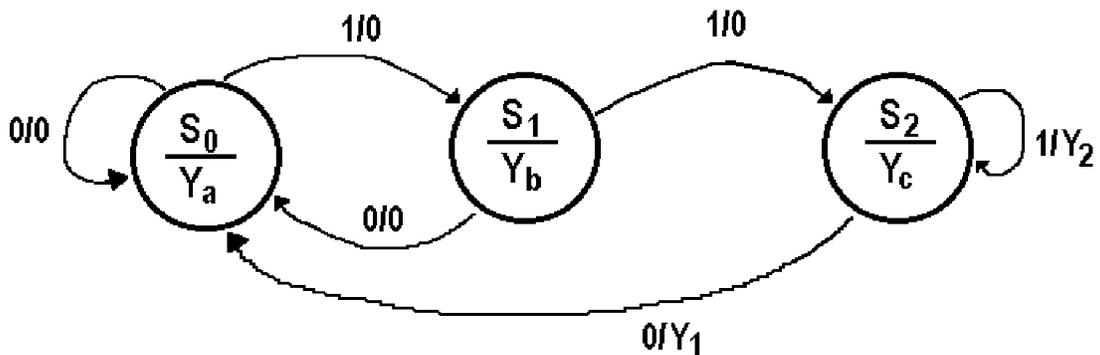
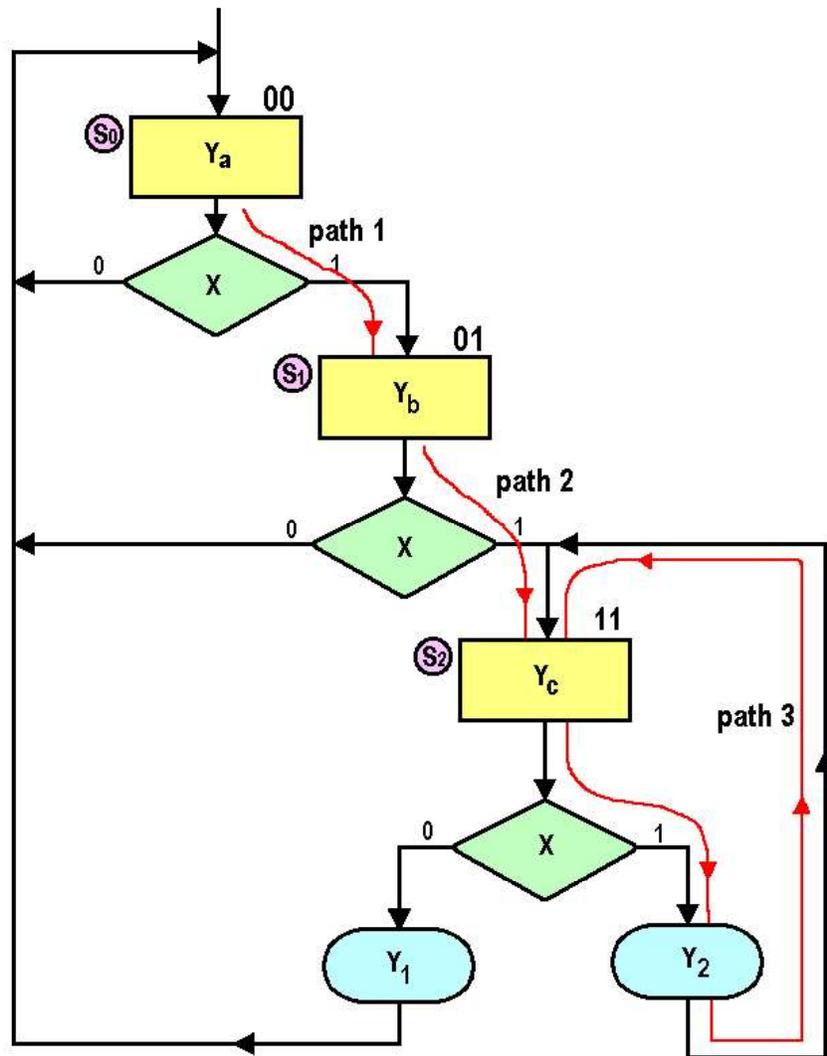


Figure 12.8: A state diagram

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The ASM chart of the state diagram shall then be as shown in Fig. 12.9.



**Figure 12.9:** ASM chart of state diagram shown in Fig. 12.8

After entering to state  $S_0$ , the output  $Y_a$  becomes “1”. State  $S_0$  will change to state  $S_1$  only when condition of input  $X = “1”$  and output  $Y_b$  will become “1”. If  $X = “0”$  then the state remains unchanged and output becomes 0.

State  $S_1$  will change to state  $S_2$  only when condition of input  $X = “1”$  and output  $Y_c$  becomes “1”. If  $X = “0”$  then state  $S_1$  will transition back to state  $S_0$ . Thus, one can see that output  $Y_c$  is always “1”.

If  $X = “1”$  and  $Y_2 = “1”$  then the state  $S_2$  remains unchanged. If  $X = “0”$  and output  $Y_1 = “1”$ , then state changes to  $S_0$ .

## 12.4 Design the Circuit with ASM Chart

The Boolean expression of the outputs shall be determined from the type, the state conditions, and input conditions that used to obtain them.

The next state equation for the flip-flop Q shall be obtained from the following procedure.

- Identify all the states in which  $Q = "1"$ .
- For each of these states, find all the link paths that lead into the state.
- For each of these link paths, find a term that is "1" when the path is followed. That is for a link path from  $S_i$  to  $S_j$ , the term will be "1" if the machine is in state  $S_i$  and the conditions for exiting to  $S_j$  are satisfied.
- The Boolean expression for next state flip-flop output  $Q^+$  is formed by ORing together the states found in above step.

We shall use the ASM chart shown in Fig. 12.8 to derive the Boolean expressions for the outputs and next state equations this sequential network.

The assignment of the state shall be  $S_0 = \bar{A} \cdot \bar{B} = "00"$ ,  $S_1 = \bar{A} \cdot B = "01"$ , and  $S_2 = A \cdot B = "11"$ . Note that A is the MSB, whilst B is LSB.

Since the Moore output  $Y_a$  and  $Y_b$  are only present state dependent, therefore, the output  $Y_a = \bar{A} \cdot \bar{B}$ ,  $Y_b = \bar{A} \cdot B$  and  $Y_c = A \cdot B$ .

The Boolean expressions for Mealy output shall be  $Y_1 = A \cdot B \cdot \bar{X}$  and  $Y_2 = A \cdot B \cdot X$ .

Following the procedure listed above link path 1, 2 and 3 are identified for determining the next state equation for the flip-flop.

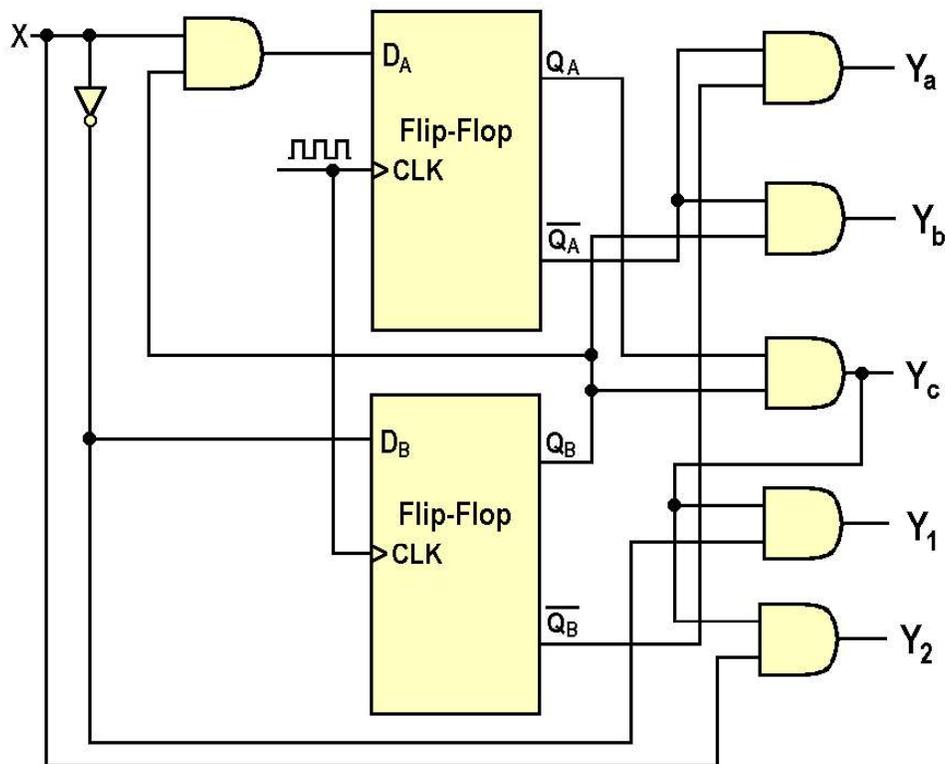
Let's begin with LSB bit B. Path 1 has B transition from "0" to "1". Thus, the Boolean expression for this transition is  $\bar{A} \cdot \bar{B} \cdot X$ . For path 2, B is transition from "1" to "1". Thus, the Boolean expression for this path is  $\bar{A} \cdot B \cdot X$ . For path 3, B is also transition from "1" to "1". Thus, its Boolean expression is  $A \cdot B \cdot X$ . ORing these Boolean expressions shall form the next state  $B^+$  equation for the LSB of the flip-flop. Thus, the next state equation for LSB B is  $B^+ = \bar{A} \cdot \bar{B} \cdot X + \bar{A} \cdot B \cdot X + A \cdot B \cdot X$ .

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For Path 1, A is transition from “0” to “0”, which does not lead to  $Q = “1”$ . Thus, it is not necessary to obtain the Boolean expression for this path. For path 2, A is transition from “0” to “1”. Its Boolean expression shall be  $\bar{A} \cdot B \cdot X$ . For path 3, A is transition from “1” to “1”. Its Boolean expression is  $A \cdot B \cdot X$ . ORing all these Boolean expressions shall form the next state  $A^+$  equation for the MSB A of flip-flop. The next state equation for A shall be  $A^+ = \bar{A} \cdot B \cdot X + A \cdot B \cdot X$ .

Now that we have obtained all the necessary Boolean expressions and next state equations. A state table can then be obtained. Deciding the flip-flop type to be used, obtaining next input of flip-flop, using optimization technique to reduce the state, and finally draw the circuit diagram.

The design using D flip-flop is shown in Fig. 12.10. Student is encouraged to list the state table from the state equations.



**Figure 12.10:** The design of the system from ASM chart shown in Fig. 12.9

Let's consider another example of design using ASM chart.

A start signal S starts the system by clearing a 4-bit binary counter A ( $A_3$ ,  $A_2$ ,  $A_1$ , and  $A_0$ ) and flip-flop F. With the next clock pulse the counter is

incremented. The counter continues to be incremented until the operation stop. The counter bit  $A_3$  and  $A_2$  are used to control the sequence.

If  $A_2 = 0$  flip-flop E is cleared and continues counting.

If  $A_2 = 1$  flip-flop E is set.

If  $A_3 = 0$  the count continues.

If  $A_3 = 1$  flip-flop F is set on next clock pulse and the system stop counting.

Based on the design statement, the ASM chart for system is shown in Fig. 12.11.

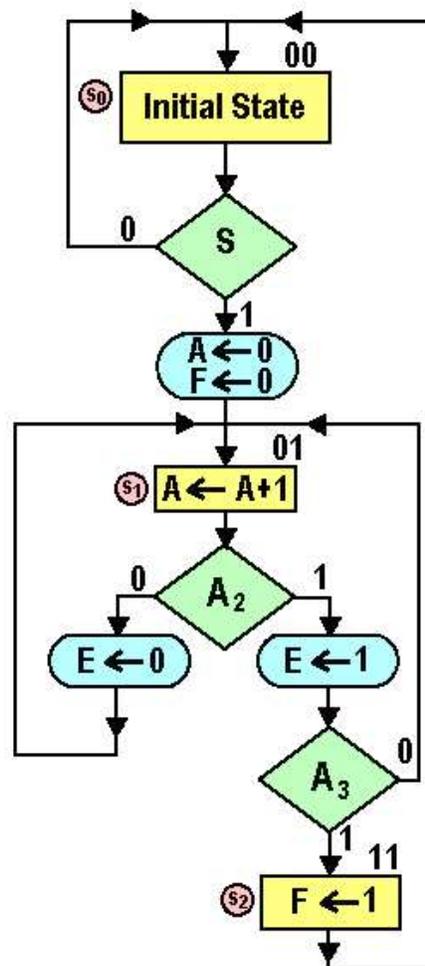


Figure 12.11: ASM chart of the design example

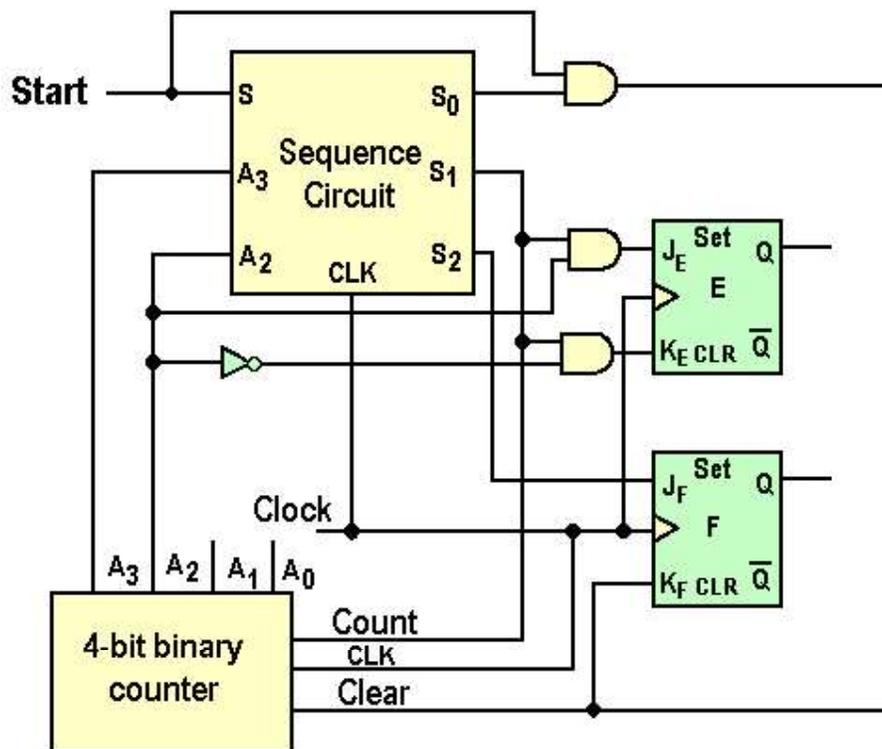
Based on the ASM chart, the flip-flop F and binary counter are reset by Boolean expression  $\bar{B} \cdot \bar{C} \cdot S$ , whereby B is the MSB and C is LSB of state. Flip E is set by Boolean expression  $\bar{B} \cdot C \cdot A_2$  and reset by Boolean expression  $\bar{B} \cdot C \cdot \bar{A}_2$ .

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Flip-flop F is set by Boolean expression  $B \cdot C$ . The binary counter is incremented by Boolean expression  $\bar{B} \cdot C$ .

If JK flip-flops are used as the flip-flop E and F, then the J input of flip-flop E is  $J_E = \bar{B} \cdot C \cdot A_2$ . The K input of flip-flop E is  $K_E = \bar{B} \cdot C \cdot \bar{A}_2$ . The J input of flip-flop F is  $J_F = B \cdot C$ . The K input of flip-flop F is  $K_F = \bar{B} \cdot \bar{C} \cdot S$ .

The block diagram of the design is shown in Fig. 12.12.



**Figure 12.12:** Block diagram of the system design for ASM shown in Fig. 12.11

The sequence circuit is designed based on the procedure listed at the beginning of this section.

The next state equation for bit B is  $B^+ = \bar{B} \cdot C \cdot A_2 \cdot A_3$ , which is shown by the red path in Fig. 12.13.

There are four paths shown in blue in Fig. 12.13 for the next state equation of bit C. Thus, the next state equation for bit C is  $C^+ = \bar{B} \cdot \bar{C} \cdot S + \bar{B} \cdot C \cdot A_2 \cdot \bar{A}_3 + \bar{B} \cdot C \cdot A_2 \cdot A_3 + \bar{B} \cdot C \cdot \bar{A}_2$ .

Based on the above results, the next-state and output state table is shown in Fig. 12.14.

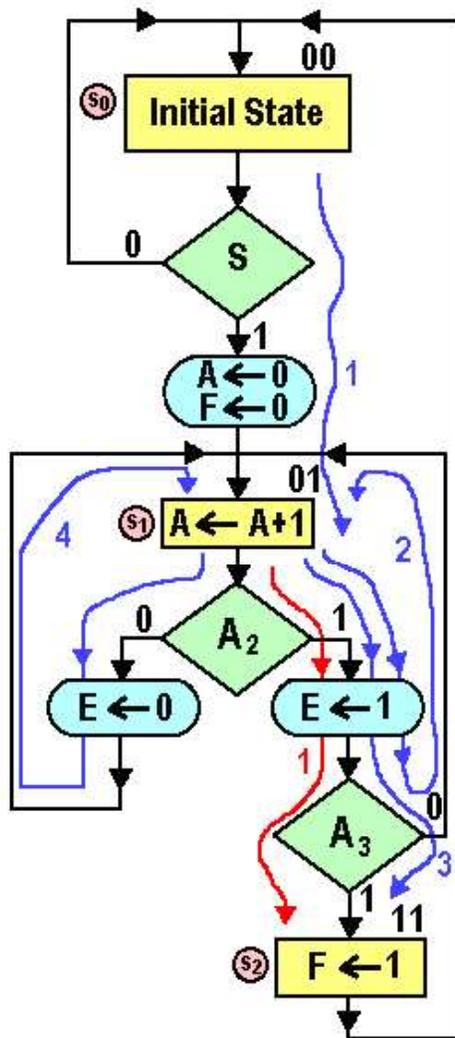


Figure 12.13: The next state paths of ASM shown in Fig. 12.11

Present State	Present State		Input			Next State		Output			
	B	C	S	A <sub>2</sub>	A <sub>3</sub>	B <sup>+</sup>	C <sup>+</sup>	J <sub>E</sub>	K <sub>E</sub>	J <sub>F</sub>	K <sub>F</sub>
S <sub>0</sub>	0	0	0	X	X	0	0	0	0	0	0
S <sub>0</sub>	0	0	1	X	X	0	1	0	0	0	1
S <sub>1</sub>	0	1	X	0	X	0	1	0	1	0	0
S <sub>1</sub>	0	1	X	1	0	0	1	1	0	0	0
S <sub>1</sub>	0	1	X	1	1	1	1	1	0	0	0
S <sub>2</sub>	1	1	X	X	X	0	0	0	0	1	0
X	1	0	X	X	X	X	X	X	X	X	X

Figure 12.14: The next-state and output state table

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If the sequencer circuit is designed using D-flip flop then the input  $D_C$  of flip-flop C shall be  $D_C = \bar{B} \cdot \bar{C} \cdot S + \bar{B} \cdot C \cdot A_2 \cdot \bar{A}_3 + \bar{B} \cdot C \cdot A_2 \cdot A_3 + \bar{B} \cdot C \cdot \bar{A}_2 = \bar{B} \cdot \bar{C} \cdot S + \bar{B} \cdot C$  and for input  $D_B$  of flip-flop B shall be  $D_B = \bar{B} \cdot C \cdot A_2 \cdot A_3$ .

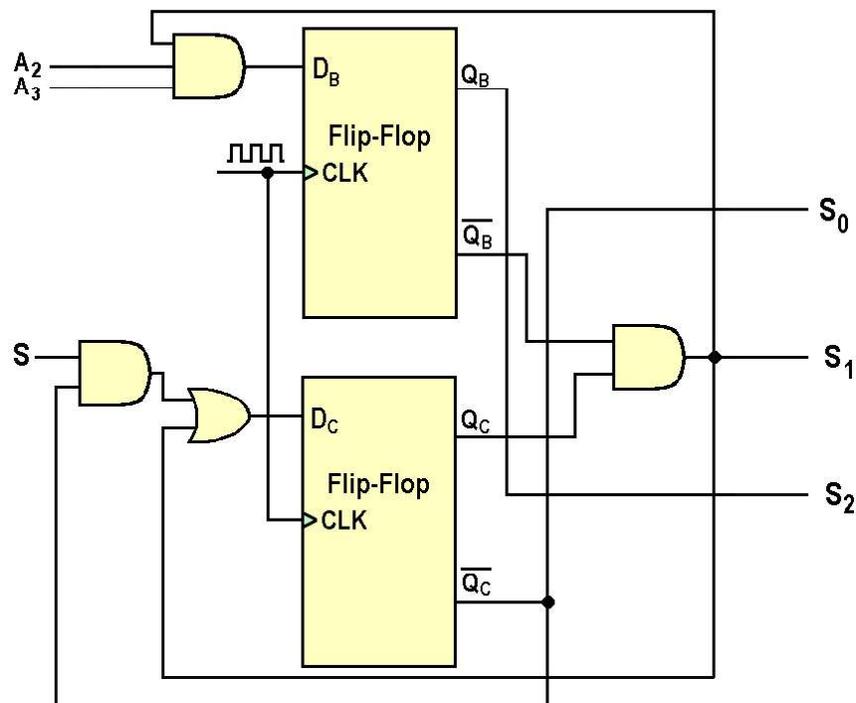
The state “10” is a don’t care state, the state table of output  $S_0$ ,  $S_1$  and  $S_2$  are shown in Fig. 12.15.

Input		Output		
B	C	$S_0$	$S_1$	$S_2$
0	0	1	0	0
0	1	0	1	0
1	0	X	X	X
1	1	0	0	1

**Figure 12.15:** State table of output  $S_0$ ,  $S_1$ , and  $S_2$

Based on the state table shown in Fig. 12.15, the Boolean expressions for  $S_0$ ,  $S_1$ , and  $S_2$  are respectively equal to  $S_0 = \bar{C}$ ,  $S_1 = \bar{B} \cdot C$ , and  $S_2 = B$ .

The design of the sequencer circuit shall then be as shown in Fig. 12.16.



**Figure 12.16:** The circuit design of sequencer circuit