10 Operational Amplifiers

CHAPTER OBJECTIVES

- Understand what a differential amplifier does
- Learn the basics of an operational amplifier
- Develop an understanding of what common mode operation is
- Describe double-ended input operation

10.1 INTRODUCTION

An operational amplifier, or op-amp, is a very high gain differential amplifier with high input impedance and low output impedance. Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, filter circuits, and many types of instrumentation circuits. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain.

Figure 10.1 shows a basic op-amp with two inputs and one output as would result using a differential amplifier input stage. Each input results in either the same or an opposite polarity (or phase) output, depending on whether the signal is applied to the plus (+) or the minus (−) input, respectively.

Single-Ended Input

Single-ended input operation results when the input signal is connected to one input with the other input connected to ground. Figure 10.2 shows the signals connected for this operation. In Fig. 10.2a, the input is applied to the plus input (with minus input at ground), which results in an output having the same polarity as the applied input signal. Figure 10.2b shows an input signal applied to the minus input, the output then being opposite in phase to the applied signal.

Double-Ended (Differential) Input

In addition to using only one input, it is possible to apply signals at each input—this being a double-ended operation. Figure 10.3a shows an input, V_d, applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the plus and minus inputs. Figure 10.3b shows the same action resulting when two separate signals are applied to the inputs, the difference signal being $V_{i_1} - V_{i_2}$.

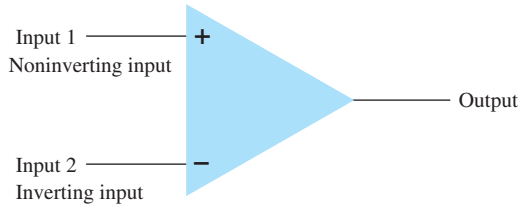


FIG. 10.1
Basic op-amp.

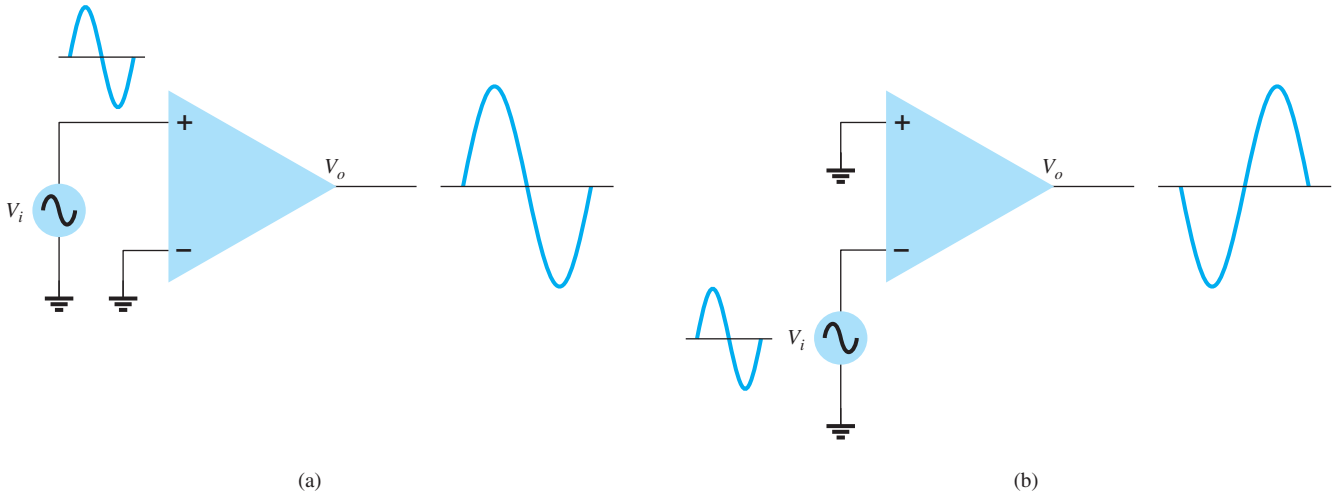


FIG. 10.2
Single-ended operation.

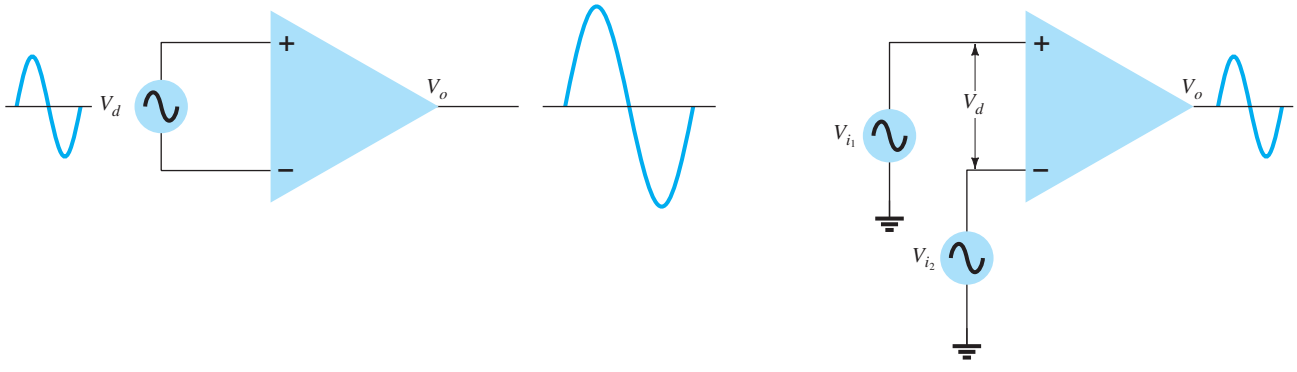


FIG. 10.3
Double-ended (differential) operation.

Double-Ended Output

Whereas the operation discussed so far has a single output, the op-amp can also be operated with opposite outputs, as shown in Fig. 10.4. An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity. Figure 10.5 shows a single-ended input with a double-ended output. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity. Figure 10.6 shows the same operation with a single output measured between output terminals (not with respect to ground). This difference output signal is $V_{o_1} - V_{o_2}$. The difference output is also referred to as a *floating signal* since neither output terminal is the ground (reference) terminal. The difference output is twice as large as either V_{o_1} or V_{o_2} because they are of opposite polarity and subtracting them results in twice their amplitude

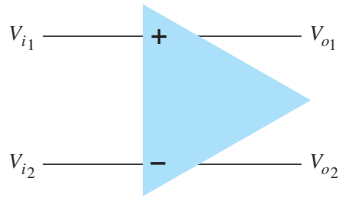


FIG. 10.4
Double-ended input with double-ended output.

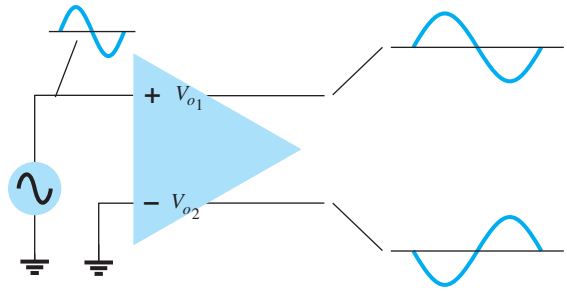


FIG. 10.5
Single-ended input with double-ended output.

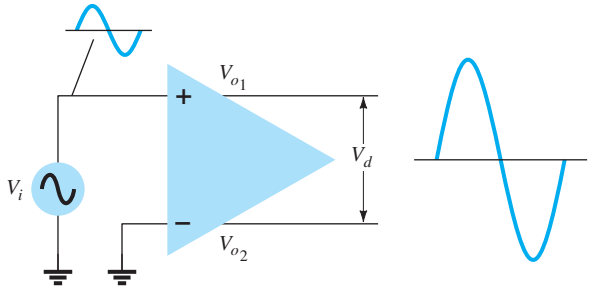


FIG. 10.6
Differential-output.

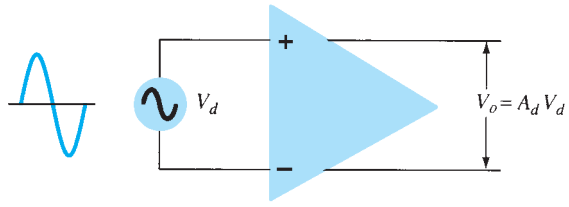


FIG. 10.7
Differential-input, differential-output operation.

[e.g., 10 V − (−10 V) = 20 V]. Figure 10.7 shows a differential input, differential output operation. The input is applied between the two input terminals and the output taken from between the two output terminals. This is fully differential operation.

Common-Mode Operation

When the same input signals are applied to both inputs, common-mode operation results, as shown in Fig. 10.8. Ideally, the two inputs are equally amplified, and since they result in opposite-polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.

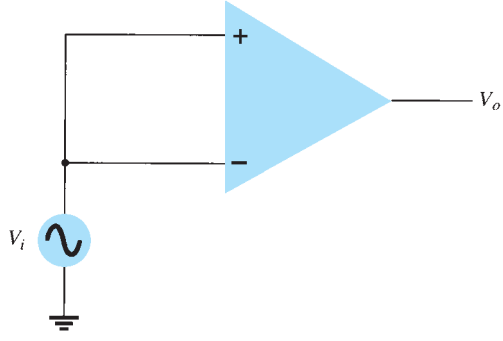


FIG. 10.8
Common-mode operation.

Common-Mode Rejection

A significant feature of a differential connection is that the signals that are opposite at the inputs are highly amplified, whereas those that are common to the two inputs are only slightly amplified—the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs. Since noise (any unwanted input signal) is generally common to both inputs, the differential connection tends to provide attenuation

of this unwanted input while providing an amplified output of the difference signal applied to the inputs. This operating feature is referred to as *common-mode rejection*.

10.2 DIFFERENTIAL AMPLIFIER CIRCUIT

The differential amplifier circuit is an extremely popular connection used in IC units. This connection can be described by considering the basic differential amplifier shown in Fig. 10.9. Notice that the circuit has two separate inputs and two separate outputs, and that the emitters are connected together. Whereas many differential amplifier circuits use two separate voltage supplies, the circuit can also operate using a single supply.

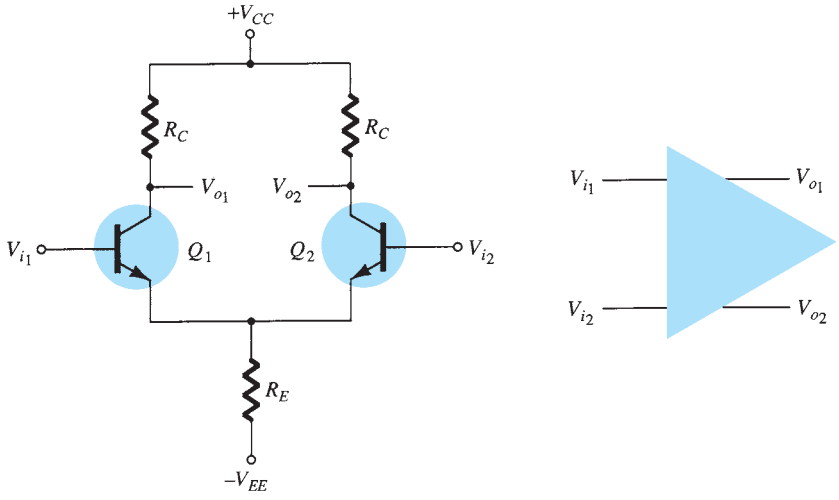


FIG. 10.9
Basic differential amplifier circuit.

A number of input signal combinations are possible:

If an input signal is applied to either input with the other input connected to ground, the operation is referred to as "single-ended."

If two opposite-polarity input signals are applied, the operation is referred to as "double-ended."

If the same input is applied to both inputs, the operation is called "common-mode."

In single-ended operation, a single input signal is applied. However, due to the common-emitter connection, the input signal operates both transistors, resulting in output from *both* collectors.

In double-ended operation, two input signals are applied, the difference of the inputs resulting in outputs from both collectors due to the difference of the signals applied to both inputs.

In common-mode operation, the common input signal results in opposite signals at each collector, these signals canceling, so that the resulting output signal is zero. As a practical matter, the opposite signals do not completely cancel, and a small signal results.

The main feature of the differential amplifier is the very large gain when opposite signals are applied to the inputs as compared to the very small gain resulting from common inputs. The ratio of this difference gain to the common gain is called *common-mode rejection.*

DC Bias

Let's first consider the dc bias operation of the circuit of Fig. 10.9. With ac inputs obtained from voltage sources, the dc voltage at each input is essentially connected to 0 V, as shown in Fig. 10.10. With each base voltage at 0 V, the common-emitter dc bias voltage is

$$V_E = 0\text{ V} - V_{BE} = -0.7\text{ V}$$

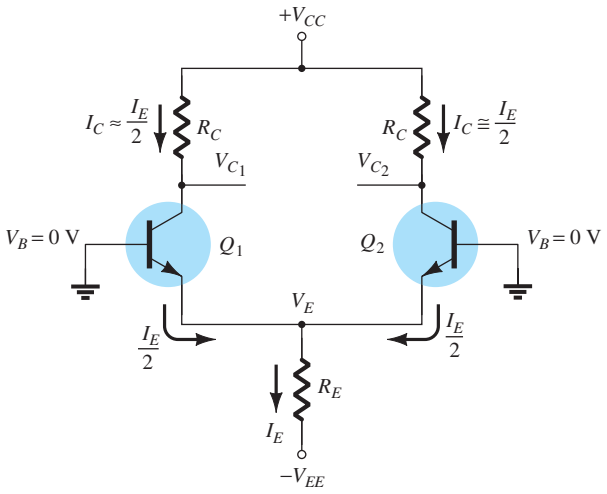


FIG. 10.10
DC bias of differential amplifier circuit.

The emitter dc bias current is then

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx \frac{V_{EE} - 0.7\text{ V}}{R_E} \tag{10.1}$$

Assuming that the transistors are well matched (as would occur in an IC unit), we obtain

$$I_{C_1} = I_{C_2} = \frac{I_E}{2} \tag{10.2}$$

resulting in a collector voltage of

$$V_{C_1} = V_{C_2} = V_{CC} - I_C R_C = V_{CC} - \frac{I_E}{2} R_C \tag{10.3}$$

EXAMPLE 10.1 Calculate the dc voltages and currents in the circuit of Fig. 10.11.

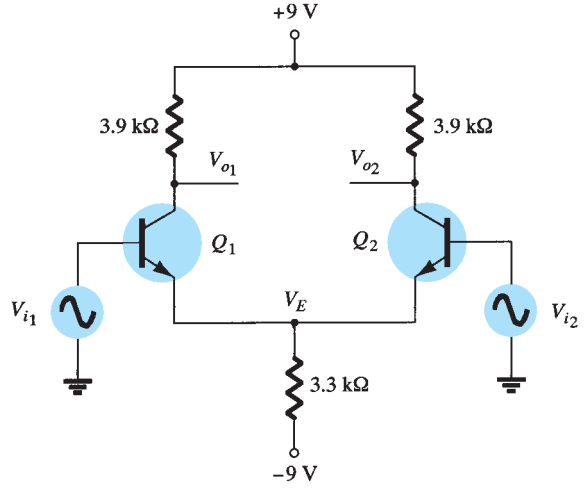


FIG. 10.11
Differential amplifier circuit for Example 10.1.

Solution:

$$\text{Eq. (10.1):} \quad I_E = \frac{V_{EE} - 0.7\text{ V}}{R_E} = \frac{9\text{ V} - 0.7\text{ V}}{3.3\text{ k}\Omega} \approx \mathbf{2.5\text{ mA}}$$

The collector current is then

$$\text{Eq. (10.2):} \quad I_C = \frac{I_E}{2} = \frac{2.5\text{ mA}}{2} = \mathbf{1.25\text{ mA}}$$

resulting in a collector voltage of

$$\text{Eq. (10.3):} \quad V_C = V_{CC} - I_C R_C = 9\text{ V} - (1.25\text{ mA})(3.9\text{ k}\Omega) \approx \mathbf{4.1\text{ V}}$$

The common-emitter voltage is thus –0.7 V, whereas the collector bias voltage is near 4.1 V for both outputs.

AC Operation of Circuit

An ac connection of a differential amplifier is shown in Fig. 10.12. Separate input signals are applied as V_{i_1} and V_{i_2}, with separate outputs resulting as V_{o_1} and V_{o_2}. To carry out ac analysis, we redraw the circuit in Fig. 10.13. Each transistor is replaced by its ac equivalent.

Single-Ended AC Voltage Gain To calculate the single-ended ac voltage gain, V_o/V_i, apply signal to one input with the other connected to ground, as shown in Fig. 10.14. The

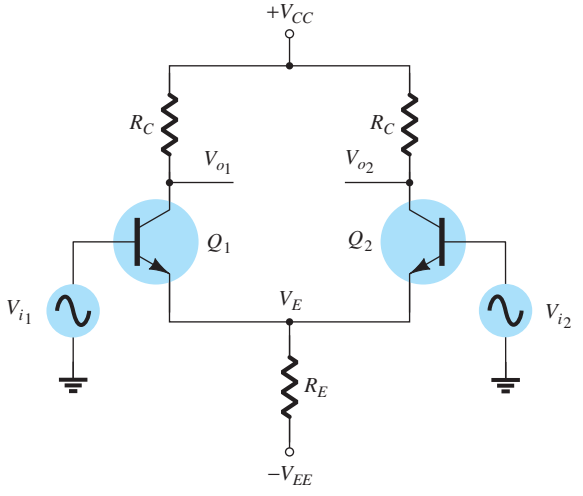


FIG. 10.12
AC connection of differential amplifier.

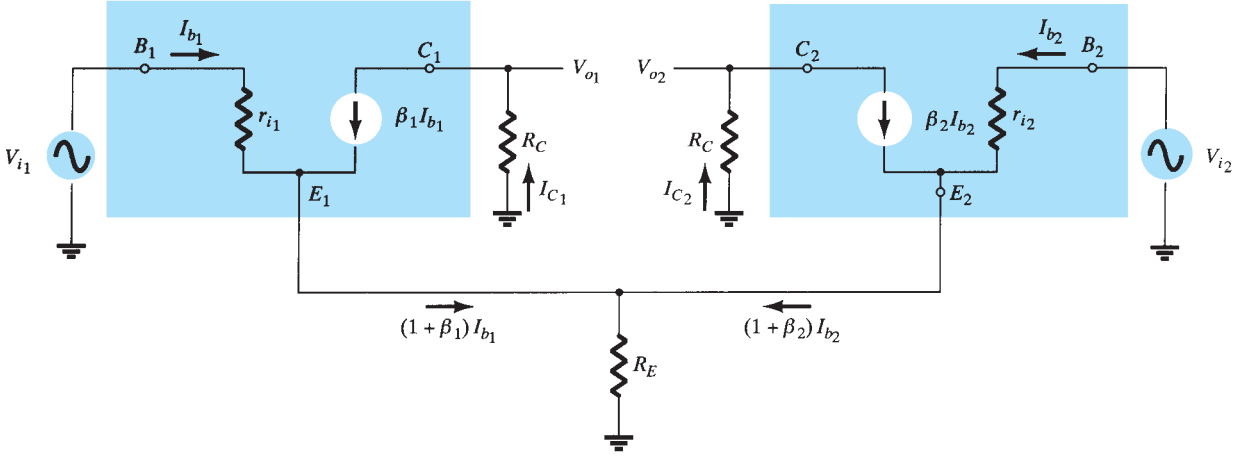


FIG. 10.13
AC equivalent of differential amplifier circuit.

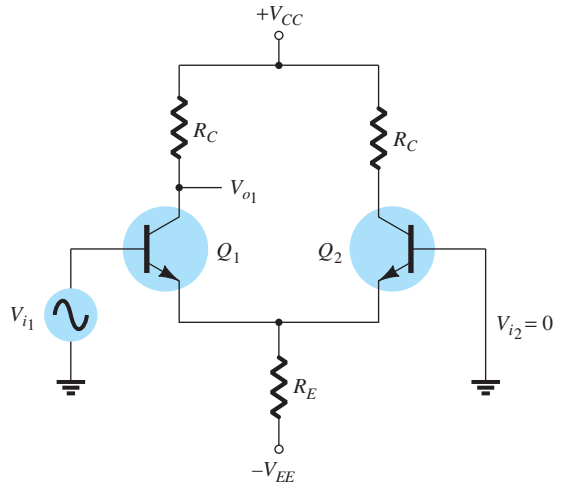


FIG. 10.14
Connection to calculate $A_{V_1} = V_{o_1}/V_{i_1}$.

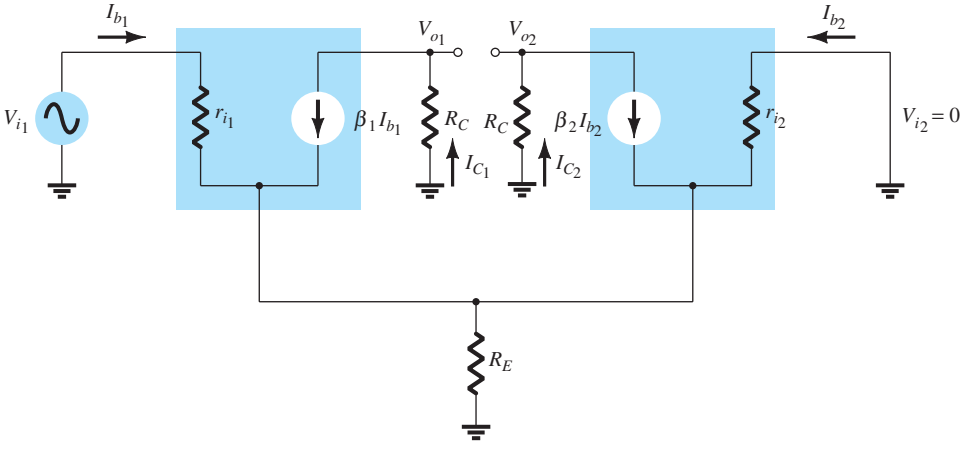


FIG. 10.15
AC equivalent of circuit in Fig. 10.14.

ac equivalent of this connection is drawn in Fig. 10.15. The ac base current can be calculated using the base 1 input Kirchhoff voltage loop (KVL) equation. If one assumes that the two transistors are well matched, then

$$I_{b_1} = I_{b_2} = I_b$$
$$r_{i_1} = r_{i_2} = r_i = \beta r_e$$

With R_E very large (ideally infinite), the circuit for obtaining the KVL equation simplifies to that of Fig. 10.16, from which we can write

$$V_{i_1} - I_b r_i - I_b r_i = 0$$

so that

$$I_b = \frac{V_{i_1}}{2r_i} = \frac{V_i}{2\beta r_e}$$

If we also assume that

$$\beta_1 = \beta_2 = \beta$$

then

$$I_C = \beta I_b = \beta \frac{V_i}{2\beta r_e} = \frac{V_i}{2r_e}$$

and the output voltage magnitude at either collector is

$$V_o = I_C R_C = \frac{V_i}{2r_e} R_C = \frac{R_C}{2r_e} V_i$$

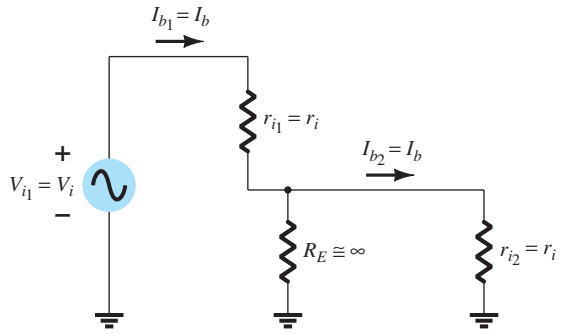


FIG. 10.16
Partial circuit for calculating I_b.

for which the single-ended voltage gain magnitude at either collector is

$$A_v = \frac{V_o}{V_i} = \frac{R_C}{2r_e} \tag{10.4}$$

EXAMPLE 10.2 Calculate the single-ended output voltage V_{o_1} for the circuit of Fig. 10.17.

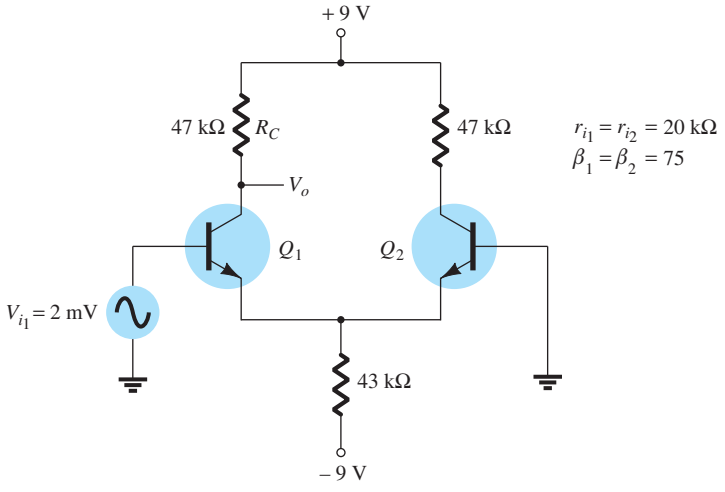


FIG. 10.17
Circuit for Examples 10.2 and 10.3.

Solution: The dc bias calculations provide

$$I_E = \frac{V_{EE} - 0.7\text{ V}}{R_E} = \frac{9\text{ V} - 0.7\text{ V}}{43\text{ k}\Omega} = 193\ \mu\text{A}$$

The collector dc current is then

$$I_C = \frac{I_E}{2} = 96.5\ \mu\text{A}$$

so that $$V_C = V_{CC} - I_C R_C = 9\text{ V} - (96.5\ \mu\text{A})(47\text{ k}\Omega) = 4.5\text{ V}$$

The value of r_e is then

$$r_e = \frac{26}{0.0965} \cong 269\ \Omega$$

The ac voltage gain magnitude can be calculated using Eq. (10.31):

$$A_v = \frac{R_C}{2r_e} = \frac{(47\ \text{k}\Omega)}{2(269\ \Omega)} = 87.4$$

providing an output ac voltage of magnitude

$$V_o = A_v V_i = (87.4)(2\ \text{mV}) = 174.8\ \text{mV} = \mathbf{0.175\ V}$$

Double-Ended AC Voltage Gain A similar analysis can be used to show that for the condition of signals applied to both inputs, the differential voltage gain magnitude is

$$A_d = \frac{V_o}{V_d} = \frac{R_C}{r_e} \tag{10.5}$$

where $V_d = V_{i_1} - V_{i_2}$.

Common-Mode Operation of Circuit

Whereas a differential amplifier provides large amplification of the difference signal applied to both inputs, it should also provide as small an amplification of the signal common to both inputs. An ac connection showing common input to both transistors is shown in Fig. 10.18. The ac equivalent circuit is drawn in Fig. 10.19, from which we can write

$$I_b = \frac{V_i - 2(\beta + 1)I_b R_E}{r_i}$$

which can be rewritten as

$$I_b = \frac{V_i}{r_i + 2(\beta + 1)R_E}$$

The output voltage magnitude is then

$$V_o = I_C R_C = \beta I_b R_C = \frac{\beta V_i R_C}{r_i + 2(\beta + 1)R_E}$$

providing a voltage gain magnitude of

$$A_c = \frac{V_o}{V_i} = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E} \tag{10.6}$$

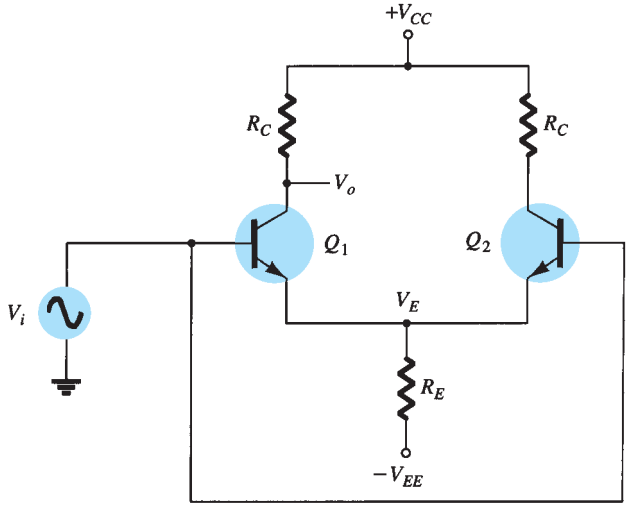


FIG. 10.18
Common-mode connection.

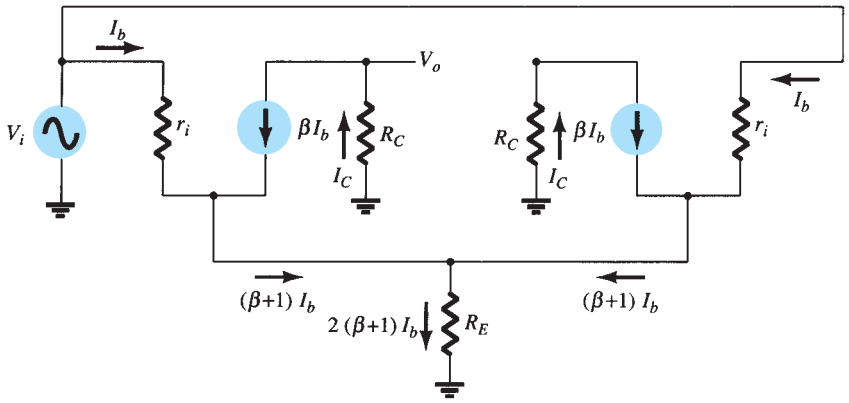


FIG. 10.19
AC circuit in common-mode connection.

EXAMPLE 10.3 Calculate the common-mode gain for the amplifier circuit of Fig. 10.17.

Solution:

$$\text{Eq. (10.6):} \quad A_c = \frac{V_o}{V_i} = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E} = \frac{75(47\,\text{k}\Omega)}{20\,\text{k}\Omega + 2(76)(43\,\text{k}\Omega)} = \mathbf{0.54}$$

Use of Constant-Current Source

A good differential amplifier has a very large difference gain A_d, which is much larger than the common-mode gain A_c. The common-mode rejection ability of the circuit can be considerably improved by making the common-mode gain as small as possible (ideally, 0). From Eq. (10.6), we see that the larger R_E, the smaller is A_c. One popular method for increasing the ac value of R_E is using a constant-current source circuit. Figure 10.20 shows a differential amplifier with constant-current source to provide a large value of resistance from common emitter to ac ground. The major improvement of this circuit over that in Fig. 10.9 is the much larger ac impedance for R_E obtained using the constant-current source. Figure 10.21 shows the ac equivalent circuit for the circuit of Fig. 10.20. A practical constant-current source is shown as a high impedance, in parallel with the constant current.

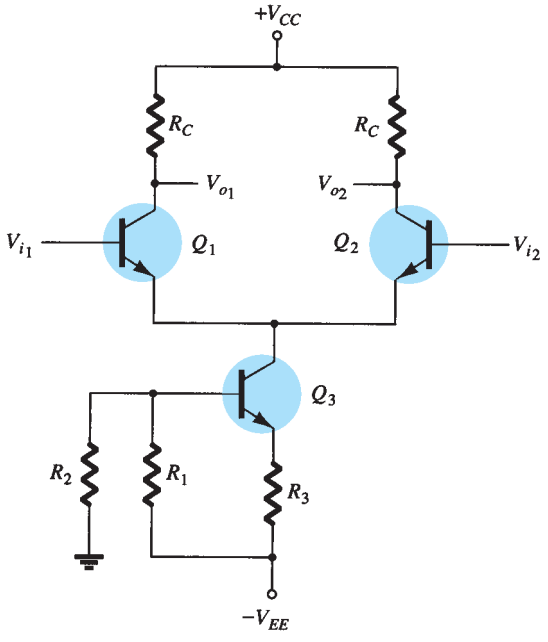


FIG. 10.20
Differential amplifier with constant-current source.

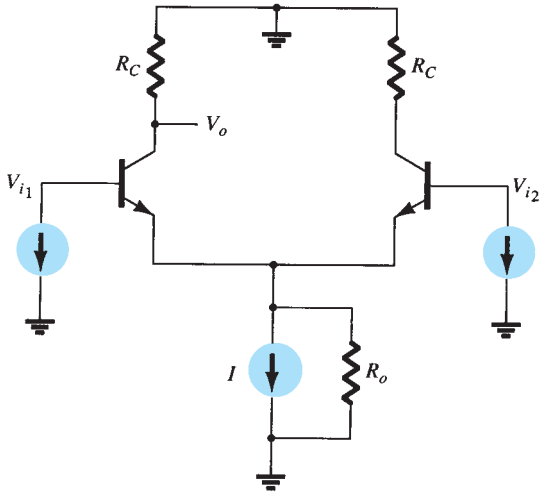


FIG. 10.21
AC equivalent of the circuit of Fig. 10.20.

EXAMPLE 10.4 Calculate the common-mode gain for the differential amplifier of Fig. 10.22.

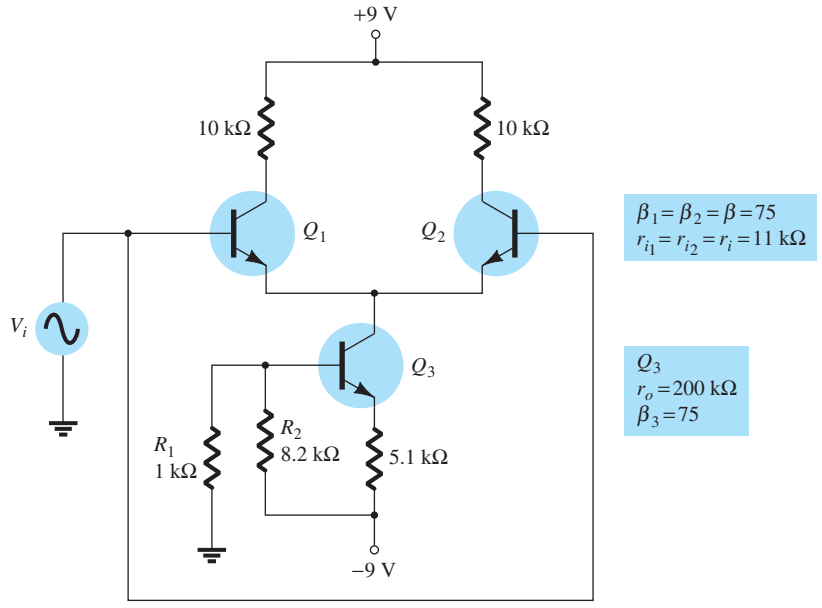


FIG. 10.22
Circuit for Example 10.4.

Solution: Using $R_E = r_o = 200\,\text{k}\Omega$ gives

$$A_c = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E} = \frac{75(10\,\text{k}\Omega)}{11\,\text{k}\Omega + 2(76)(200\,\text{k}\Omega)} = \mathbf{24.7 \times 10^{-3}}$$

10.3 BiFET, BiMOS, AND CMOS DIFFERENTIAL AMPLIFIER CIRCUITS

Whereas the preceding section provided an introduction to the differential amplifier using bipolar devices, units commercially available also use JFET and MOSFET transistors to build these types of circuits. An IC unit containing a differential amplifier built using both bipolar (Bi) and junction field-effect (FET) transistors is referred to as a *BiFET circuit.* An IC unit made using both bipolar (Bi) and MOSFET (MOS) transistors is called a *BiMOS circuit.* Finally, a circuit built using opposite-type MOSFET transistors is a *CMOS circuit.*

The CMOS is a form of circuit popular in digital circuitry and uses both *n*-channel and *p*-channel enhancement MOSFET transistors (see Fig. 10.23). This complementary MOSFET or CMOS circuit uses these opposite (or complementary)-type transistors. The input V_i is applied to both gates with the output taken from the connected drains. Before going into the operation of the CMOS circuit, let's review the operation of the enhancement MOSFET transistors.

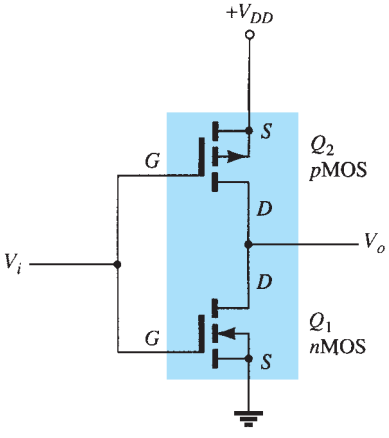


FIG. 10.23
CMOS inverter circuit.

*n*MOS On/Off Operation

The drain characteristic of an *n*-channel enhancement MOSFET or *n*MOS transistor is shown in Fig. 10.24a. With 0 V applied to the gate–source, there is no drain current. Not until V_{GS} is raised past the device threshold level V_T does any current result. With an input of, say, +5 V, the *n*MOS device is fully on with current I_D present. In summary:

An input of 0 V leaves the nMOS "off," whereas an input of +5V turns the nMOS on.

*p*MOS On/Off Operation

The drain characteristic for a *p*-channel MOSFET or *p*MOS transistor is shown in Fig. 10.24b. When 0 V is applied, the device is "off" (no drain current present), whereas for an

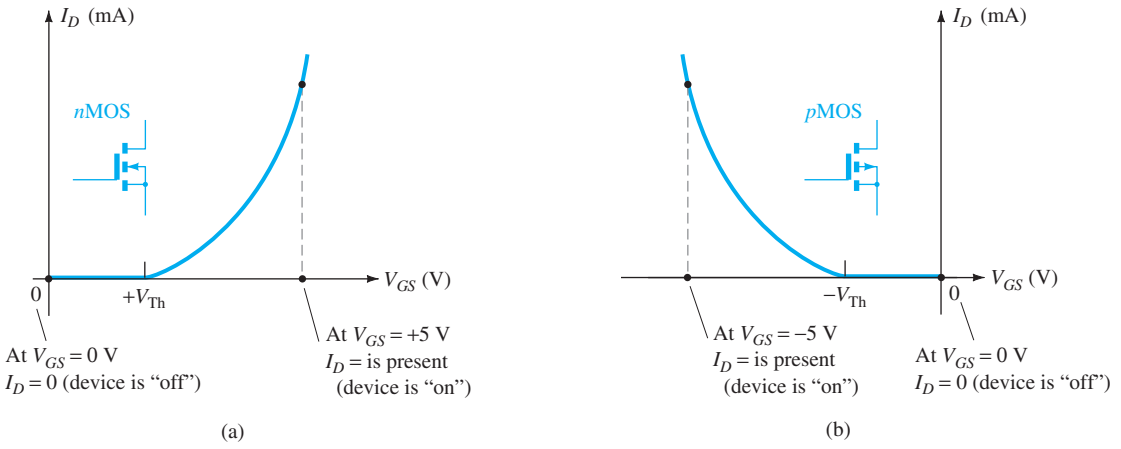


FIG. 10.24

Enhancement MOSFET characteristic showing off and on conditions: (a) nMOS; (b) pMOS.

input of −5 V (greater than the threshold voltage), the device is "on" with drain current present. In summary:

$V_{GS} = 0$ V leaves pMOS "off;" $V_{GS} = -5$ V turns pMOS on.

Consider next how the actual CMOS circuit of Fig. 10.25 operates for input of 0 V or +5 V.

0-V Input

When 0 V is applied as input to the CMOS circuit, it provides 0 V to both *n*MOS and *p*MOS gates. Figure 10.25a shows that

$$\text{For } n\text{MOS } (Q_1): \quad V_{GS} = V_i - 0\text{ V} = 0\text{ V} - 0\text{ V} = 0\text{ V}$$

$$\text{For } p\text{MOS } (Q_2): \quad V_{GS} = V_i - (+5\text{ V}) = 0\text{ V} - 5\text{ V} = -5\text{ V}$$

Input of 0 V to an *n*MOS transistor Q_1 leaves that device "off." The same 0-V input, however, results in the gate–source voltage of *p*MOS transistor Q_2 being −5 V (gate at 0 V is 5 V less than source at +5 V), resulting in that device turning on. The output, V_o, is then +5 V.

+5-V Input

When $V_i = +5$ V, it provides +5 V to both gates. Figure 10.25b shows that

$$\text{For } n\text{MOS } (Q_1): \quad V_{GS} = V_i - 0\text{ V} = +5\text{ V} - 0\text{ V} = +5\text{ V}$$

$$\text{For } p\text{MOS } (Q_2): \quad V_{GS} = V_i - (+5\text{ V}) = +5\text{ V} - 5\text{ V} = 0\text{ V}$$

This input results in transistor Q_1 being turned on and transistor Q_2 remaining off, the output then near 0 V, through conducting transistor Q_2. The CMOS connection of Fig. 10.23 provides operation as a logic inverter with V_o the opposite of V_i, as shown in Table 10.1.

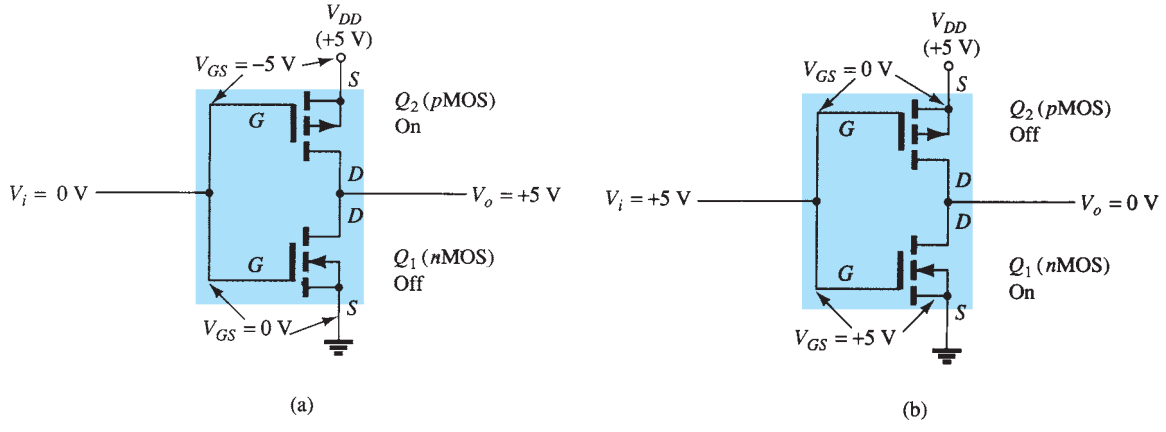


FIG. 10.25

Operation of CMOS circuit: (a) output +5 V; (b) output 0 V.

TABLE 10.1
Operation of CMOS Circuit

V_i (V)	Q_1	Q_2	V_o (V)
0	Off	On	+5
+5	On	Off	0

The circuits used below to show the various multidevice circuits are mostly symbolic, since the actual circuits used in ICs are much more complex. Figure 10.26 shows a BiFET circuit with JFET transistors at the inputs and bipolar transistors to provide the current source (using a current mirror circuit). The current mirror ensures that each JFET is operated at the same bias current. For ac operation, the JFET provides a high input impedance (much higher than that provided using only bipolar transistors).

Figure 10.27 shows a circuit using MOSFET input transistors and bipolar transistors for the current sources, the BiMOS unit providing even higher input impedance than the BiFET due to the use of MOSFET transistors.

Finally, a differential amplifier circuit can be built using complementary MOSFET transistors as shown in Fig. 10.28. The *p*MOS transistors provide the opposite inputs, whereas the *n*MOS transistors operate as the constant-current source. A single output is taken from

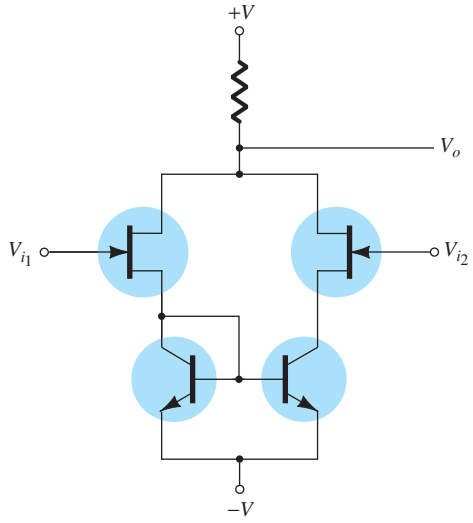


FIG. 10.26
BiFET differential amplifier circuit.

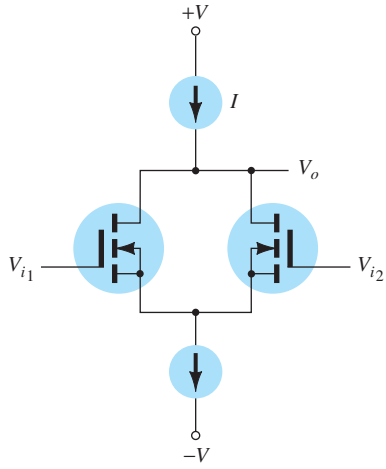


FIG. 10.27
BiMOS differential amplifier circuit.

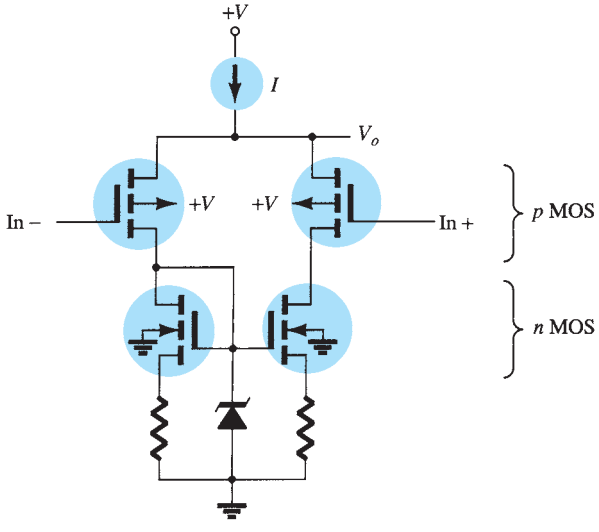


FIG. 10.28
CMOS differential amplifier.

the common point between *n*MOS and *p*MOS transistors on one side of the circuit. This type of CMOS differential amplifier is particularly well suited for battery operation due to the low power dissipation of a CMOS circuit.

10.4 OP-AMP BASICS

An operational amplifier is a very high gain amplifier having very high input impedance (typically a few megohms) and low output impedance (less than 100 Ω). The basic circuit is made using a difference amplifier having two inputs (plus and minus) and at least one output. Figure 10.29 shows a basic op-amp unit. As discussed earlier, the plus (+) input produces an output that is in phase with the signal applied, whereas an input to the minus (−) input results in an opposite-polarity output. The ac equivalent circuit of the op-amp is shown in Fig. 10.30a. As shown, the input signal applied between input terminals sees an input impedance R_i that is typically very high. The output voltage is shown to be the amplifier gain times the input signal taken through an output impedance R_o, which is typically very low. An ideal op-amp circuit, as shown in Fig. 10.30b, would have infinite input impedance, zero output impedance, and infinite voltage gain.

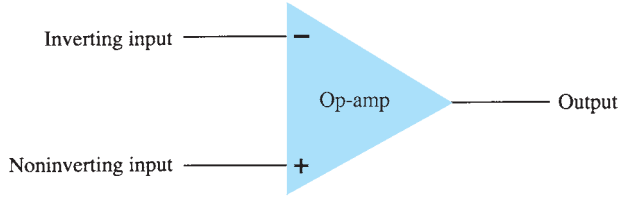


FIG. 10.29
Basic op-amp.

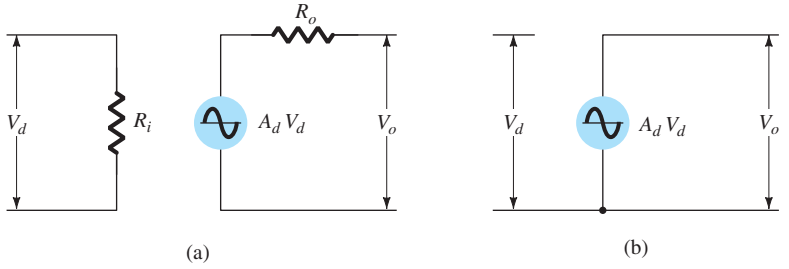


FIG. 10.30
AC equivalent of op-amp circuit: (a) practical; (b) ideal.

Basic Op-Amp

The basic circuit connection using an op-amp is shown in Fig. 10.31. The circuit shown provides operation as a constant-gain multiplier. An input signal V_1 is applied through resistor R_1 to the minus input. The output is then connected back to the same minus input through resistor R_f. The plus input is connected to ground. Since the signal V_1 is essentially applied to the minus input, the resulting output is opposite in phase to the input signal. Figure 10.32a shows the op-amp replaced by its ac equivalent circuit. If we use the ideal

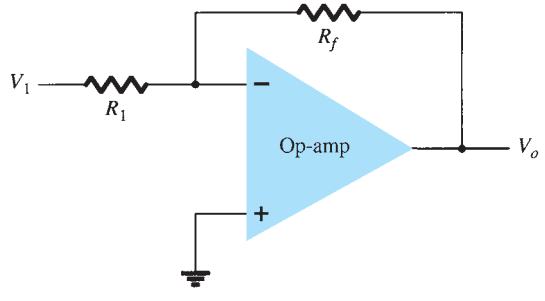


FIG. 10.31
Basic op-amp connection.

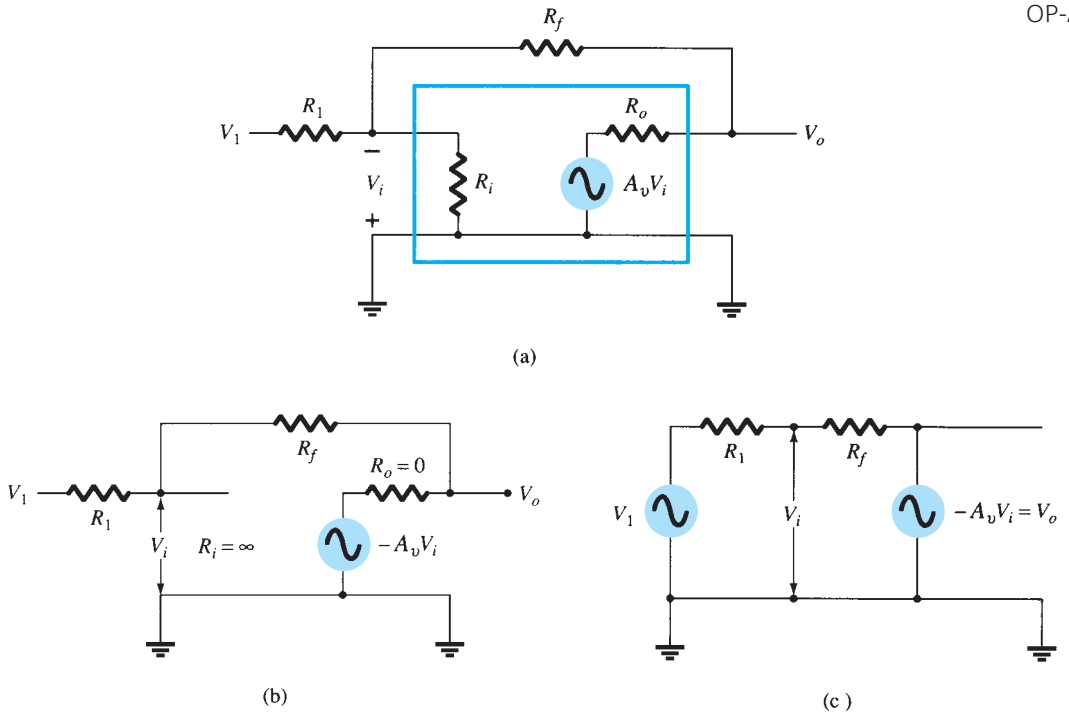


FIG. 10.32

Operation of op-amp as constant-gain multiplier: (a) op-amp ac equivalent circuit; (b) ideal op-amp equivalent circuit; (c) redrawn equivalent circuit.

op-amp equivalent circuit, replacing R_i by an infinite resistance and R_o by a zero resistance, the ac equivalent circuit is that shown in Fig. 10.32b. The circuit is then redrawn, as shown in Fig. 10.32c, from which circuit analysis is carried out.

Using superposition, we can solve for the voltage V_1 in terms of the components due to each of the sources. For source V_1 only ($-A_vV_i$ set to zero),

$$V_{i_1} = \frac{R_f}{R_1 + R_f}V_1$$

For source $-A_vV_i$ only (V_1 set to zero),

$$V_{i_2} = \frac{R_1}{R_1 + R_f}(-A_vV_i)$$

The total voltage V_i is then

$$V_i = V_{i_1} + V_{i_2} = \frac{R_f}{R_1 + R_f}V_1 + \frac{R_1}{R_1 + R_f}(-A_vV_i)$$

which can be solved for V_i as

$$V_i = \frac{R_f}{R_f + (1 + A_v)R_1}V_1 \qquad \textbf{(10.7)}$$

If $A_v \gg 1$ and $A_v R_1 \gg R_f$, as is usually true, then

$$V_i = \frac{R_f}{A_vR_1}V_1$$

Solving for V_o/V_i, we get

$$\frac{V_o}{V_i} = \frac{-A_vV_i}{V_i} = \frac{-A_v}{V_i}\frac{R_fV_1}{A_vR_1} = -\frac{R_f}{R_1}\frac{V_1}{V_i}$$

so that

$$\boxed{\frac{V_o}{V_1} = -\frac{R_f}{R_1}} \qquad \textbf{(10.8)}$$

The result in Eq. (10.8) shows that the ratio of overall output to input voltage is dependent only on the values of resistors R_1 and R_f—provided that A_v is very large.

Unity Gain

If $R_f = R_1$, the gain is

$$\text{Voltage gain} = -\frac{R_f}{R_1} = -1$$

so that the circuit provides a unity voltage gain with 180° phase inversion. If R_f is exactly R_1, the voltage gain is exactly 1.

Constant-Magnitude Gain

If R_f is some multiple of R_1, the overall amplifier gain is a constant. For example, if $R_f = 10R_1$, then

$$\text{Voltage gain} = -\frac{R_f}{R_1} = -10$$

and the circuit provides a voltage gain of exactly 10 along with a 180° phase inversion from the input signal. If we select precise resistor values for R_f and R_1, we can obtain a wide range of gains, the gain being as accurate as the resistors used and is only slightly affected by temperature and other circuit factors.

Virtual Ground

The output voltage is limited by the supply voltage of, typically, a few volts. As stated before, voltage gains are very high. If, for example, $V_o = -10$ V and $A_v = 20{,}000$, the input voltage is

$$V_i = \frac{-V_o}{A_v} = \frac{10\text{ V}}{20{,}000} = 0.5\text{ mV}$$

If the circuit has an overall gain (V_o/V_1) of, say, 1, the value of V_1 is 10 V. Compared to all other input and output voltages, the value of V_i is then small and may be considered 0 V.

Note that although $V_i \approx 0$ V, it is not exactly 0 V. (The output voltage is a few volts due to the very small input V_i times a very large gain A_v.) The fact that $V_i \approx 0$ V leads to the concept that at the amplifier input there exists a virtual short-circuit or virtual ground.

The concept of a virtual short implies that although the voltage is nearly 0 V, there is no current through the amplifier input to ground. Figure 10.33 depicts the virtual ground concept. The heavy line is used to indicate that we may consider that a short exists with $V_i \approx 0$ V but that this is a virtual short so that no current goes through the short to ground. Current goes only through resistors R_1 and R_f as shown.

Using the virtual ground concept, we can write equations for the current I as follows:

$$I = \frac{V_1}{R_1} = -\frac{V_o}{R_f}$$

which can be solved for V_o/V_1:

$$\frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

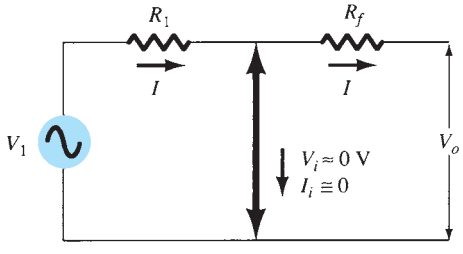


FIG. 10.33
Virtual ground in an op-amp.

The virtual ground concept, which depends on A_v being very large, allowed a simple solution to determine the overall voltage gain. It should be understood that although the circuit of Fig. 10.33 is not physically correct, it does allow an easy means for determining the overall voltage gain.

10.5 PRACTICAL OP-AMP CIRCUITS

The op-amp can be connected in a large number of circuits to provide various operating characteristics. In this section, we cover a few of the most common of these circuit connections.

Inverting Amplifier

The most widely used constant-gain amplifier circuit is the inverting amplifier, as shown in Fig. 10.34. The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor (R_1) and feedback resistor (R_f)—this output also being inverted from the input. Using Eq. (10.8), we can write

$$V_o = -\frac{R_f}{R_1} V_1$$

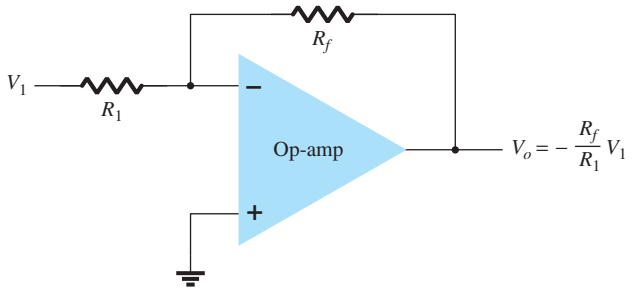


FIG. 10.34
Inverting constant-gain multiplier.

EXAMPLE 10.5 If the circuit of Fig. 10.34 has $R_1 = 100\,\text{k}\Omega$ and $R_f = 500\,\text{k}\Omega$, what output voltage results for an input of $V_1 = 2\,\text{V}$?

Solution:

$$\text{Eq. (10.8):} \quad V_o = -\frac{R_f}{R_1} V_1 = -\frac{500\,\text{k}\Omega}{100\,\text{k}\Omega}(2\,\text{V}) = \mathbf{-10\,V}$$

Noninverting Amplifier

The connection of Fig. 10.35a shows an op-amp circuit that works as a noninverting amplifier or constant-gain multiplier. It should be noted that the inverting amplifier connection is more widely used because it has better frequency stability (discussed later). To determine the voltage gain of the circuit, we can use the equivalent representation shown in Fig. 10.35b. Note that the voltage across R_1 is V_1 since $V_i \approx 0\,\text{V}$. This must be equal to the output voltage, through a voltage divider of R_1 and R_f, so that

$$V_1 = \frac{R_1}{R_1 + R_f} V_o$$

which results in

$$\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \qquad \textbf{(10.9)}$$

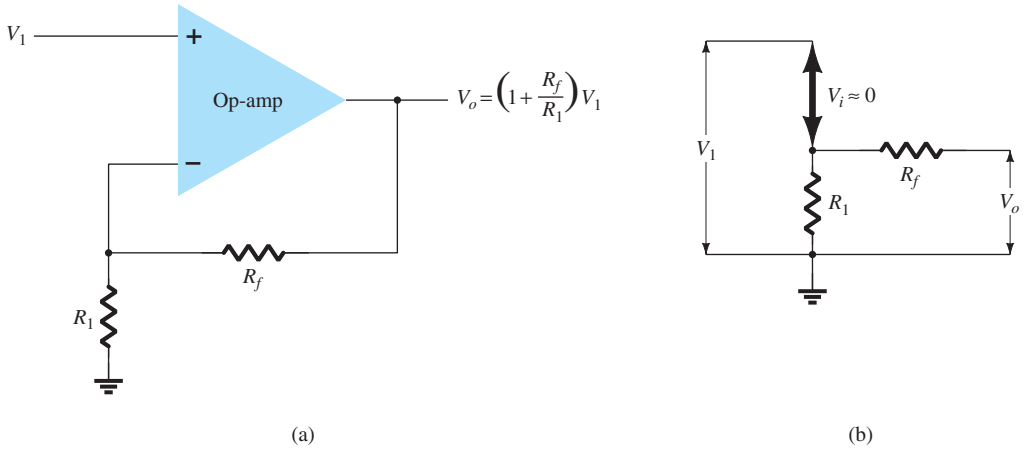


FIG. 10.35
Noninverting constant-gain multiplier.

EXAMPLE 10.6 Calculate the output voltage of a noninverting amplifier (as in Fig. 10.35) for values of $V_1 = 2$ V, $R_f = 500\ \text{k}\Omega$, and $R_1 = 100\ \text{k}\Omega$.

Solution:

$$\text{Eq. (10.9):} \quad V_o = \left(1 + \frac{R_f}{R_1}\right) V_1 = \left(1 + \frac{500\ \text{k}\Omega}{100\ \text{k}\Omega}\right)(2\ \text{V}) = 6(2\ \text{V}) = \mathbf{+12\ V}$$

Unity Follower

The unity-follower circuit, as shown in Fig. 10.36a, provides a gain of unity (1) with no polarity or phase reversal. From the equivalent circuit (see Fig. 10.36b) it is clear that

$$\boxed{V_o = V_1} \qquad \textbf{(10.10)}$$

and that the output is the same polarity and magnitude as the input. The circuit operates like an emitter- or source-follower circuit except that the gain is exactly unity.

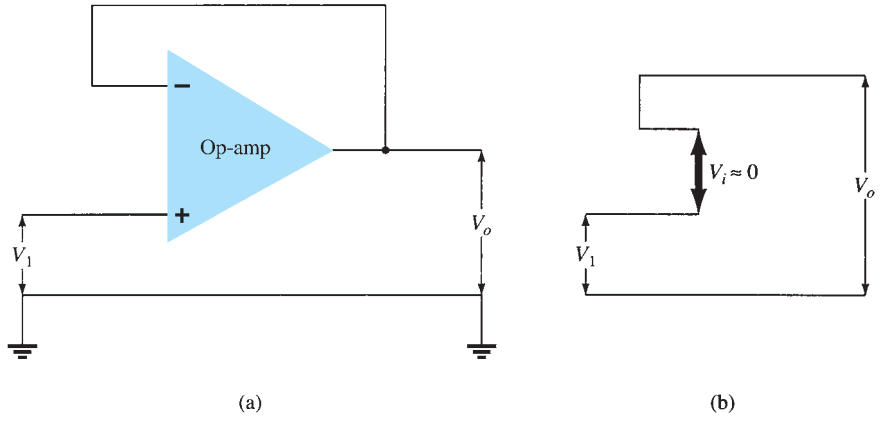


FIG. 10.36
(a) Unity follower; (b) virtual-ground equivalent circuit.

Summing Amplifier

Probably the most used of the op-amp circuits is the summing amplifier circuit shown in Fig. 10.37a. The circuit shows a three-input summing amplifier circuit, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain

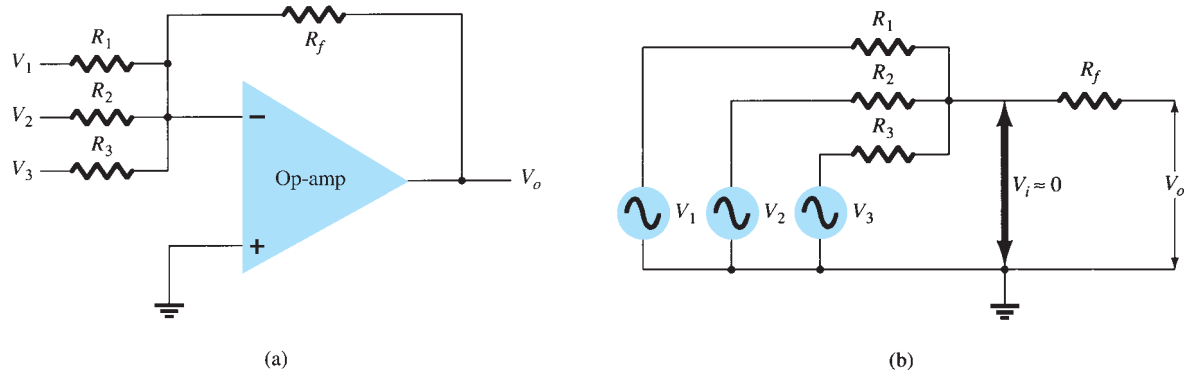


FIG. 10.37

(a) Summing amplifier; (b) virtual-ground equivalent circuit.

factor. Using the equivalent representation shown in Fig. 10.37b, we can express the output voltage in terms of the inputs as

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) \tag{10.11}$$

In other words, each input adds a voltage to the output multiplied by its separate constant-gain multiplier. If more inputs are used, they each add an additional component to the output.

EXAMPLE 10.7 Calculate the output voltage of an op-amp summing amplifier for the following sets of voltages and resistors. Use $R_f = 1\ \text{M}\Omega$ in all cases.

a. $V_1 = +1\ \text{V}, V_2 = +2\ \text{V}, V_3 = +3\ \text{V}, R_1 = 500\ \text{k}\Omega, R_2 = 1\ \text{M}\Omega, R_3 = 1\ \text{M}\Omega.$
b. $V_1 = -2\ \text{V}, V_2 = +3\ \text{V}, V_3 = +1\ \text{V}, R_1 = 200\ \text{k}\Omega, R_2 = 500\ \text{k}\Omega, R_3 = 1\ \text{M}\Omega.$

Solution: Using Eq. (10.11), we obtain

a. $$V_o = -\left[\frac{1000\ \text{k}\Omega}{500\ \text{k}\Omega}(+1\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+2\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+3\ \text{V})\right]$$
$$= -[2(1\ \text{V}) + 1(2\ \text{V}) + 1(3\ \text{V})] = \mathbf{-7\ V}$$

b. $$V_o = -\left[\frac{1000\ \text{k}\Omega}{200\ \text{k}\Omega}(-2\ \text{V}) + \frac{1000\ \text{k}\Omega}{500\ \text{k}\Omega}(+3\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+1\ \text{V})\right]$$
$$= -[5(-2\ \text{V}) + 2(3\ \text{V}) + 1(1\ \text{V})] = \mathbf{+3\ V}$$

Integrator

So far, the input and feedback components have been resistors. If the feedback component used is a capacitor, as shown in Fig. 10.38a, the resulting connection is called an *integrator*. The virtual-ground equivalent circuit (Fig. 10.38b) shows that an expression for the voltage between input and output can be derived in terms of the current I from input to output. Recall that virtual ground means that we can consider the voltage at the junction of R and X_C to be ground (since $V_i \approx 0\ \text{V}$) but that no current goes into ground at that point. The capacitive impedance can be expressed as

$$X_C = \frac{1}{j\omega C} = \frac{1}{sC}$$

where $s = j\omega$ is in the Laplace notation.* Solving for V_o/V_1 yields

$$I = \frac{V_1}{R} = -\frac{V_o}{X_C} = \frac{-V_o}{1/sC} = -sCV_o$$

*Laplace notation allows expressing differential or integral operations, which are part of calculus, in algebraic form using the operator s. Readers unfamiliar with calculus should ignore the steps leading to Eq. (10.13) and follow the physical meaning used thereafter.

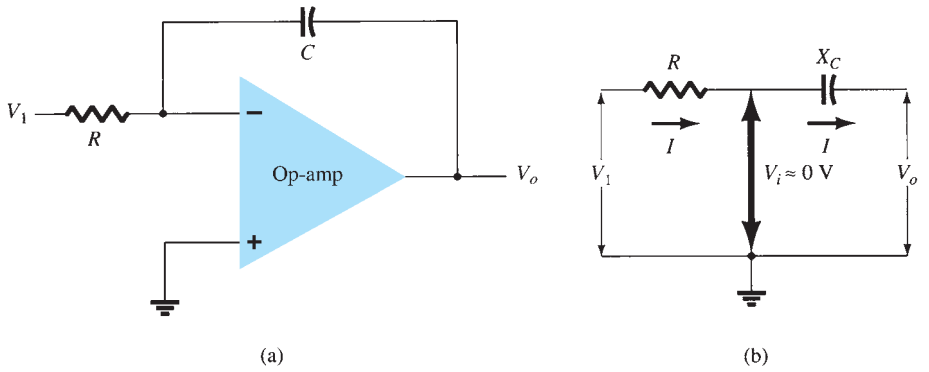


FIG. 10.38
Integrator.

$$\frac{V_o}{V_1} = \frac{-1}{sCR} \tag{10.12}$$

This expression can be rewritten in the time domain as

$$v_o(t) = -\frac{1}{RC}\int v_1(t)\,dt \tag{10.13}$$

Equation (10.13) shows that the output is the integral of the input, with an inversion and scale multiplier of $1/RC$. The ability to integrate a given signal provides the analog computer with the ability to solve differential equations and therefore provides the ability to electrically solve analogs of physical system operation.

The integration operation is one of summation, summing the area under a waveform or a curve over a period of time. If a fixed voltage is applied as input to an integrator circuit, Eq. (10.13) shows that the output voltage grows over a period of time, providing a ramp voltage. Equation (10.13) can thus be understood to show that the output voltage ramp (for a fixed input voltage) is opposite in polarity to the input voltage and is multiplied by the factor $1/RC$. Although the circuit of Fig. 10.38 can operate on many varied types of input signals, the following examples will use only a fixed input voltage, resulting in a ramp output voltage.

As an example, consider an input voltage $V_1 = 1$ V to the integrator circuit of Fig. 10.39a. The scale factor of $1/RC$ is

$$-\frac{1}{RC} = \frac{1}{(1\ \text{M}\Omega)(1\ \mu\text{F})} = -1$$

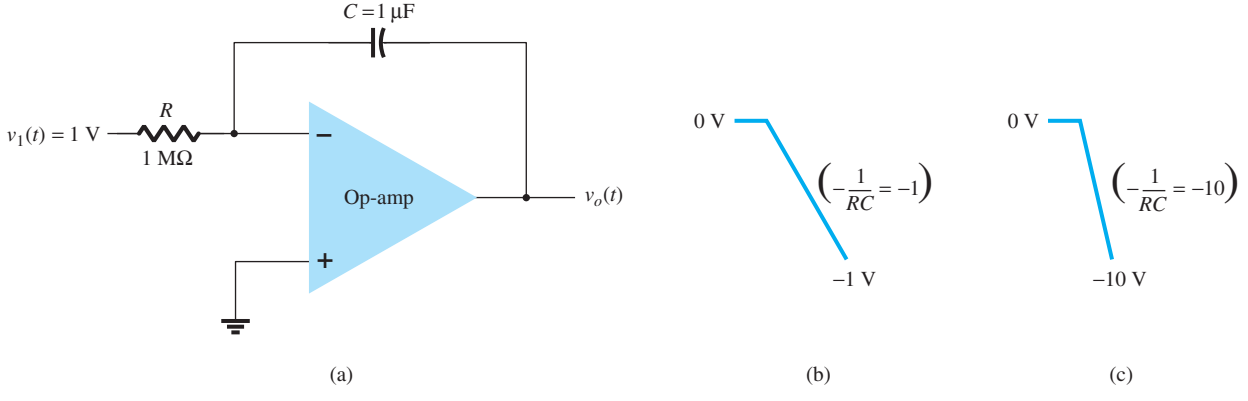


FIG. 10.39
Operation of integrator with step input.

so that the output is a negative ramp voltage as shown in Fig. 10.39b. If the scale factor is changed by making $R = 100\ \text{k}\Omega$, for example, then

$$-\frac{1}{RC} = \frac{1}{(100\ \text{k}\Omega)(1\ \mu\text{F})} = -10$$

and the output is then a steeper ramp voltage, as shown in Fig. 10.39c.

More than one input may be applied to an integrator, as shown in Fig. 10.40, with the resulting operation given by

$$v_o(t) = -\left[\frac{1}{R_1C}\int v_1(t)\,dt + \frac{1}{R_2C}\int v_2(t)\,dt + \frac{1}{R_3C}\int v_3(t)\,dt\right] \qquad \textbf{(10.14)}$$

An example of a summing integrator as used in an analog computer is given in Fig. 10.40. The actual circuit is shown with input resistors and feedback capacitor, whereas the analog-computer representation indicates only the scale factor for each input.

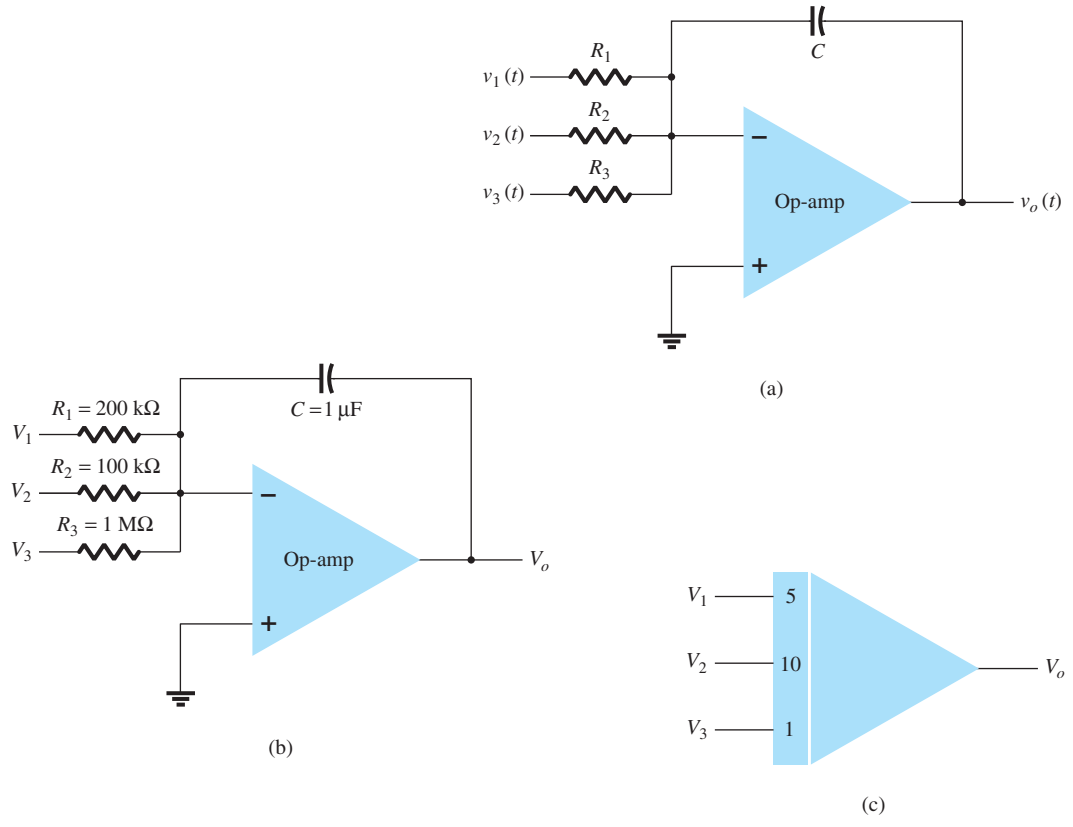


FIG. 10.40

(a) Summing-integrator circuit; (b) component values; (c) analog-computer, integrator-circuit representation.

Differentiator

A differentiator circuit is shown in Fig. 10.41. Although it is not as useful as the circuit forms covered above, the differentiator does provide a useful operation, the resulting relation for the circuit being

$$\boxed{v_o(t) = -RC\frac{dv_1(t)}{dt}} \qquad \textbf{(10.15)}$$

where the scale factor is $-RC$.

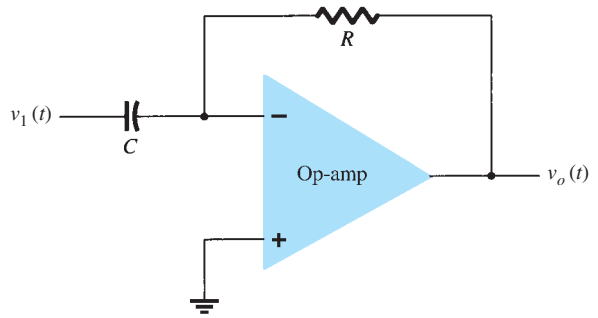


FIG. 10.41
Differentiator circuit.

10.6 OP-AMP SPECIFICATIONS–DC OFFSET PARAMETERS

Before going into various practical applications using op-amps, we should become familiar with some of the parameters used to define the operation of the unit. These specifications include both dc and transient or frequency operating features, as covered next.

Offset Currents and Voltages

Although the op-amp output should be 0 V when the input is 0 V, in actual operation there is some offset voltage at the output. For example, if one connected 0 V to both op-amp inputs and then measured 26 mV(dc) at the output, this would represent 26 mV of unwanted voltage generated by the circuit and not by the input signal. Since the user may connect the amplifier circuit for various gain and polarity operations, however, the manufacturer specifies an input offset voltage for the op-amp. The output offset voltage is then determined by the input offset voltage and the gain of the amplifier, as connected by the user.

The output offset voltage can be shown to be affected by two separate circuit conditions: (1) an input offset voltage V_{IO} and (2) an offset current due to the difference in currents resulting at the plus (+) and minus (−) inputs.

Input Offset Voltage V_{IO} The manufacturer's specification sheet provides a value of V_{IO} for the op-amp. To determine the effect of this input voltage on the output, consider the connection shown in Fig. 10.42. Using $V_o = AV_i$, we can write

$$V_o = AV_i = A\left(V_{IO} - V_o\frac{R_1}{R_1 + R_f}\right)$$

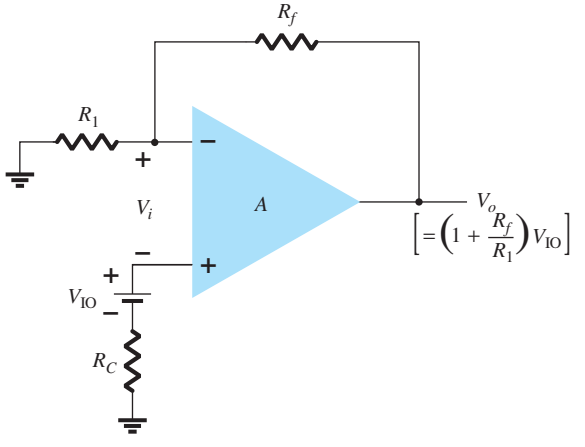


FIG. 10.42
Operation showing effect of input offset voltage V_{IO}.

Solving for V_o, we get

$$V_o = V_{IO}\frac{A}{1 + A\left[R_1/(R_1 + R_f)\right]} \approx V_{IO}\frac{A}{A\left[R_1/(R_1 + R_f)\right]}$$

from which we can write

$$V_o(\text{offset}) = V_{IO}\frac{R_1 + R_f}{R_1} \tag{10.16}$$

Equation (10.16) shows how the output offset voltage results from a specified input offset voltage for a typical amplifier connection of the op-amp.

EXAMPLE 10.8 Calculate the output offset voltage of the circuit in Fig. 10.43. The op-amp spec lists $V_{IO} = 1.2$ mV.

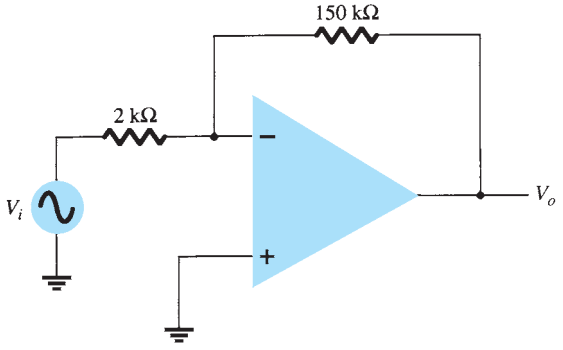


FIG. 10.43
Op-amp connection for Examples 10.8 and 10.9.

Solution:

$$\text{Eq. (10.16):} \quad V_o(\text{offset}) = V_{IO}\frac{R_1 + R_f}{R_1} = (1.2\text{ mV})\left(\frac{2\text{ k}\Omega + 150\text{ k}\Omega}{2\text{ k}\Omega}\right) = \mathbf{91.2\text{ mV}}$$

Output Offset Voltage Due to Input Offset Current I_{IO} An output offset voltage will also result due to any difference in dc bias currents at both inputs. Since the two input transistors are never exactly matched, each will operate at a slightly different current. For a typical op-amp connection, such as that shown in Fig. 10.44, an output offset voltage can be determined as follows. Replacing the bias currents through the input resistors by the voltage drop that each develops as shown in Fig. 10.45, we can determine the expression for

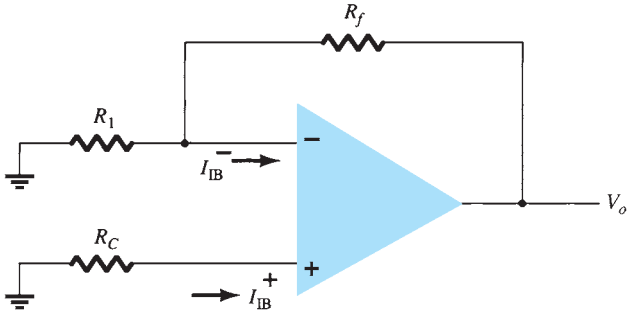


FIG. 10.44
Op-amp connection showing input bias currents.

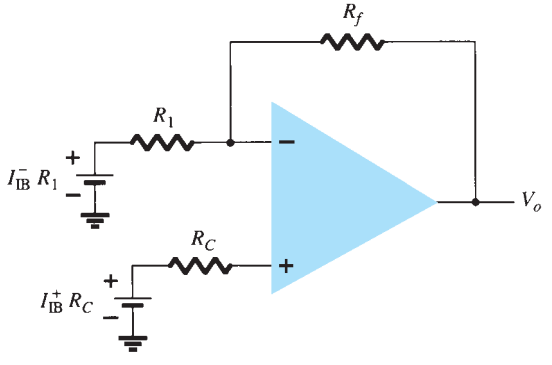


FIG. 10.45
Redrawn circuit of Fig. 10.44.

the resulting output voltage. Using superposition, we see that the output voltage due to input bias current I_{IB}^{+}, denoted by V_o^{+}, is given by

$$V_o^{+} = I_{IB}^{+} R_C\left(1 + \frac{R_f}{R_1}\right)$$

whereas the output voltage due to only I_{IB}^{-}, denoted by V_o^{-}, is given by

$$V_o^{-} = I_{IB}^{-} R_1\left(-\frac{R_f}{R_1}\right)$$

for a total output offset voltage of

$$V_o(\text{offset due to } I_{IB}^{+} \text{ and } I_{IB}^{-}) = I_{IB}^{+} R_C\left(1 + \frac{R_f}{R_1}\right) - I_{IB}^{-} R_1 \frac{R_f}{R_1} \qquad \textbf{(10.17)}$$

Since the main consideration is the difference between the input bias currents rather than each value, we define the offset current I_{IO} by

$$I_{IO} = I_{IB}^{+} - I_{IB}^{-}$$

Since the compensating resistance R_C is usually approximately equal to the value of R_1, using $R_C = R_1$ in Eq. (10.17), we can write

$$\begin{aligned} V_o(\text{offset}) &= I_{IB}^{+}(R_1 + R_f) - I_{IB}^{-} R_f \\ &= I_{IB}^{+} R_f - I_{IB}^{-} R_f = R_f(I_{IB}^{+} - I_{IB}^{-}) \end{aligned}$$

resulting in

$$\boxed{V_o(\text{offset due to } I_{IO}) = I_{IO} R_f} \qquad \textbf{(10.18)}$$

EXAMPLE 10.9 Calculate the offset voltage for the circuit of Fig. 10.43 for op-amp specification listing $I_{IO} = 100$ nA.

Solution: Eq. (10.18): $V_o = I_{IO} R_f = (100\text{ nA})(150\text{ k}\Omega) = \mathbf{15\text{ mV}}$

Total Offset Due to V_{IO} and I_{IO} Since the op-amp output may have an output offset voltage due to both factors covered above, the total output offset voltage can be expressed as

$$|V_o(\text{offset})| = |V_o(\text{offset due to} V_{IO})| + |V_o(\text{offset due to } I_{IO})| \qquad \textbf{(10.19)}$$

The absolute magnitude is used to accommodate the fact that the offset polarity may be either positive or negative.

EXAMPLE 10.10 Calculate the total offset voltage for the circuit of Fig. 10.46 for an op-amp with specified values of input offset voltage $V_{IO} = 4$ mV and input offset current $I_{IO} = 150$ nA.

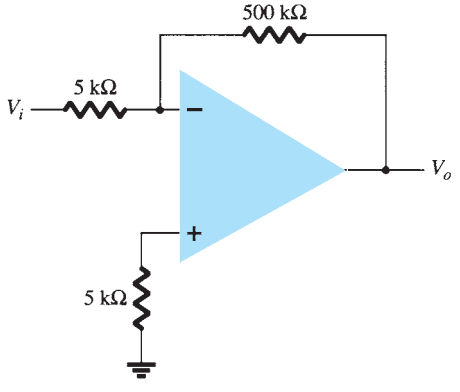


FIG. 10.46
Op-amp circuit for Example 10.10.

Solution: The offset due to V_{IO} is

$$\text{Eq. (10.16):} \quad V_o(\text{offset due to } V_{IO}) = V_{IO}\frac{R_1 + R_f}{R_1} = (4\text{ mV})\left(\frac{5\text{ k}\Omega + 500\text{ k}\Omega}{5\text{ k}\Omega}\right)$$
$$= 404\text{ mV}$$

$$\text{Eq. (10.18):} \quad V_o(\text{offset due to } I_{IO}) = I_{IO}R_f = (150\text{ nA})(500\text{ k}\Omega) = 75\text{ mV}$$

resulting in a total offset

$$\text{Eq. (10.19):} \quad V_o(\text{total offset}) = V_o(\text{offset due to } V_{IO}) + V_o(\text{offset due to } I_{IO})$$
$$= 404\text{ mV} + 75\text{ mV} = \mathbf{479\text{ mV}}$$

Input Bias Current, I_{IB} A parameter related to I_{IO} and the separate input bias currents I_{IB}^+ and I_{IB}^- is the average bias current defined as

$$I_{IB} = \frac{I_{IB}^+ + I_{IB}^-}{2} \tag{10.20}$$

One could determine the separate input bias currents using the specified values I_{IO} and I_{IB}. It can be shown that for $I_{IB}^+ > I_{IB}^-$

$$I_{IB}^+ = I_{IB} + \frac{I_{IO}}{2} \tag{10.21}$$

$$I_{IB}^- = I_{IB} - \frac{I_{IO}}{2} \tag{10.22}$$

EXAMPLE 10.11 Calculate the input bias currents at each input of an op-amp having specified values of $I_{IO} = 5$ nA and $I_{IB} = 30$ nA.

Solution: Using Eq. (10.21), we obtain

$$I_{IB}^+ = I_{IB} + \frac{I_{IO}}{2} = 30\text{ nA} + \frac{5\text{ nA}}{2} = \mathbf{32.5\text{ nA}}$$

$$I_{IB}^- = I_{IB} - \frac{I_{IO}}{2} = 30\text{ nA} - \frac{5\text{ nA}}{2} = \mathbf{27.5\text{ nA}}$$

10.7 OP-AMP SPECIFICATIONS—FREQUENCY PARAMETERS

An op-amp is designed to be a high-gain, wide-bandwidth amplifier. This operation tends to be unstable (oscillate) due to positive feedback (see Chapter 14). To ensure stable operation, op-amps are built with internal compensation circuitry, which also causes the very high open-loop gain to diminish with increasing frequency. This gain reduction is referred to as *roll-off*. In most op-amps, roll-off occurs at a rate of 20 dB per decade (−20 dB/decade) or 6 dB per octave (−6 dB/octave). (Refer to Chapter 9 for introductory coverage of dB and frequency response.)

Note that although op-amp specifications list an open-loop voltage gain (A_{VD}), the user typically connects the op-amp using feedback resistors to reduce the circuit voltage gain to a much smaller value (closed-loop voltage gain, A_{CL}). A number of circuit improvements result from this gain reduction. First, the amplifier voltage gain is a more stable, precise value set by the external resistors; second, the input impedance of the circuit is increased over that of the op-amp alone; third, the circuit output impedance is reduced from that of the op-amp alone; and finally, the frequency response of the circuit is increased over that of the op-amp alone.

Gain–Bandwidth

Because of the internal compensation circuitry included in an op-amp, the voltage gain drops off as frequency increases. Op-amp specifications provide a description of the gain versus bandwidth. Figure 10.47 provides a plot of gain versus frequency for a typical op-amp. At low frequency down to dc operation the gain is that value listed by the manufacturer's

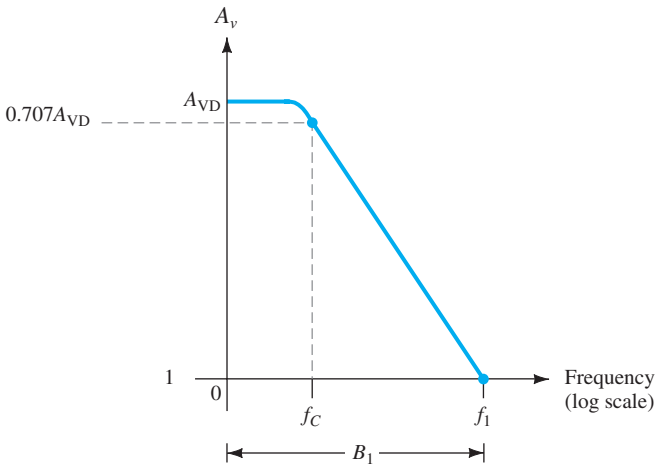


FIG. 10.47
Gain versus frequency plot.

specification A_{VD} (voltage differential gain) and is typically a very large value. As the frequency of the input signal increases, the open-loop gain drops off until it finally reaches the value of 1 (unity). The frequency at this gain value is specified by the manufacturer as the unity-gain bandwidth, B_1. Although this value is a frequency (see Fig. 10.47) at which the gain becomes 1, it can be considered a bandwidth, since the frequency band from 0 Hz to the unity-gain frequency is also a bandwidth. One could therefore refer to the point at which the gain reduces to 1 as the unity-gain frequency (f_1) or unity-gain bandwidth (B_1).

Another frequency of interest, as shown in Fig. 10.47, is that at which the gain drops by 3 dB (or to 0.707 the dc gain, A_{VD}), this being the cutoff frequency of the op-amp, f_C. In fact, the unity-gain frequency and cutoff frequency are related by

$$f_1 = A_{VD} f_C \tag{10.23}$$

Equation (10.23) shows that the unity-gain frequency may also be called the gain–bandwidth product of the op-amp.

EXAMPLE 10.12 Determine the cutoff frequency of an op-amp having specified values $B_1 = \mathbf{1\ MHz}$ and $A_{VD} = 200\ \text{V/mV}$.

Solution: Since $f_1 = B_1 = 1$ MHz, we can use Eq. (10.23) to calculate

$$f_C = \frac{f_1}{A_{VD}} = \frac{1\ \text{MHz}}{200\ \text{V/mV}} = \frac{1 \times 10^6}{200 \times 10^3} = \mathbf{5\ Hz}$$

Slew Rate (SR)

Another parameter reflecting the op-amp's ability to handle varying signals is the slew rate, defined as

Slew rate = maximum rate at which amplifier output can change in volts per microsecond (V/μs)

$$\text{SR} = \frac{\Delta V_o}{\Delta t}\ \text{V/}\mu\text{s} \quad \text{with } t \text{ in } \mu\text{s} \tag{10.24}$$

The slew rate provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal.* If one tried to drive the output at a rate

*The closed-loop gain is that obtained with the output connected back to the input in some way.

of voltage change greater than the slew rate, the output would not be able to change fast enough and would not vary over the full range expected, resulting in signal clipping or distortion. In any case, the output would not be an amplified duplicate of the input signal if the op-amp slew rate were to be exceeded.

EXAMPLE 10.13 For an op-amp having a slew rate of SR $= 2\ \text{V}/\mu\text{s}$, what is the maximum closed-loop voltage gain that can be used when the input signal varies by 0.5 V in 10 μs?

Solution: Since $V_o = A_{\text{CL}}V_i$, we can use

$$\frac{\Delta V_o}{\Delta t} = A_{\text{CL}}\frac{\Delta V_i}{\Delta t}$$

from which we get

$$A_{\text{CL}} = \frac{\Delta V_o/\Delta t}{\Delta V_i/\Delta t} = \frac{\text{SR}}{\Delta V_i/\Delta t} = \frac{2\ \text{V}/\mu\text{s}}{0.5\ \text{V}/10\ \mu\text{s}} = \mathbf{40}$$

Any closed-loop voltage gain of magnitude greater than 40 would drive the output at a rate greater than the slew rate allows, so the maximum closed-loop gain is 40.

Maximum Signal Frequency

The maximum frequency at which an op-amp may operate depends on both the bandwidth (BW) and slew rate (SR) parameters of the op-amp. For a sinusoidal signal of general form

$$v_o = K\sin(2\pi ft)$$

the maximum voltage rate of change can be shown to be

$$\text{signal maximum rate of change} = 2\pi fK\ \text{V/s}$$

To prevent distortion at the output, the rate of change must also be less than the slew rate, that is,

$$2\pi fK \le \text{SR}$$
$$\omega K \le \text{SR}$$

so that

$$\boxed{\begin{aligned} f &\le \frac{\text{SR}}{2\pi K} \quad \text{Hz} \\ \omega &\le \frac{\text{SR}}{K} \quad \text{rad/s} \end{aligned}} \qquad \textbf{(10.25)}$$

Additionally, the maximum frequency f in Eq. (10.25) is also limited by the unity-gain bandwidth.

EXAMPLE 10.14 For the signal and circuit of Fig. 10.48, determine the maximum frequency that may be used. Op-amp slew rate is SR $= 0.5\ \text{V}/\mu\text{s}$.

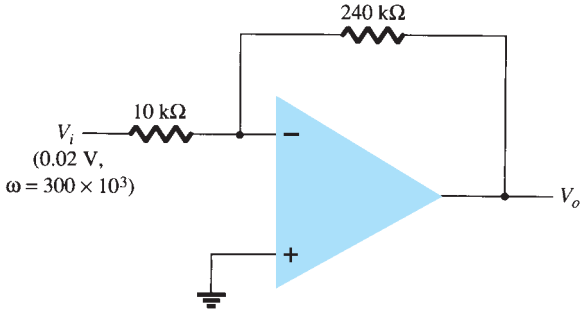


FIG. 10.48
Op-amp circuit for Example 10.14.

Solution: For a gain of magnitude

$$A_{CL} = \left|\frac{R_f}{R_1}\right| = \frac{240\ \text{k}\Omega}{10\ \text{k}\Omega} = 24$$

the output voltage provides

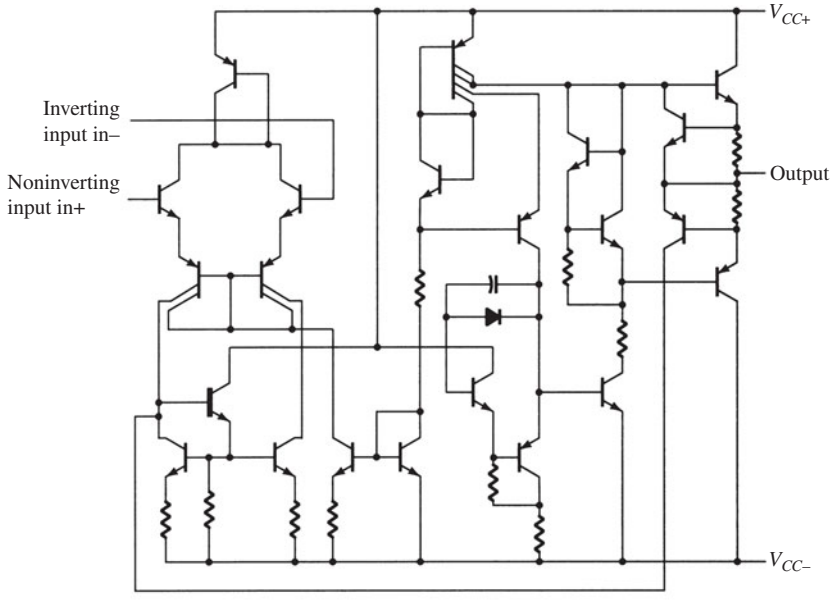
$$K = A_{CL}V_i = 24(0.02\ \text{V}) = 0.48\ \text{V}$$

Eq. (10.25): $$\omega \leq \frac{\text{SR}}{K} = \frac{0.5\ \text{V}/\mu\text{s}}{0.48\ \text{V}} = \mathbf{1.1 \times 10^6\ rad/s}$$

Since the signal frequency $\omega = 300 \times 10^3$ rad/s is less than the maximum value determined above, no output distortion will result.

10.8 OP-AMP UNIT SPECIFICATIONS

In this section, we discuss how the manufacturer's specifications are read for a typical op-amp unit. A popular bipolar op-amp IC is the 741, described by the information provided in Fig. 10.49. The op-amp is available in a number of packages, an 8-pin DIP and a 10-pin flatpack being among the more usual forms.



Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	uA741	UNIT
Supply voltage V_{CC+}	22	V
Supply voltage V_{CC-}	– 22	V
Differential input voltage	± 30	V
Input voltage any input	± 15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}	± 0.5	V
Duration of output short-circuit	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature	500	mW
Operating free-air temperature range	– 40 to 85	°C
Storage temperature range	– 65 to 150	°C
Lead temperature 1,6 mm (1/16 in.) from case for 60 seconds	300	°C
Lead temperature 1,6 mm (1/16 in.) from case for 10 seconds	260	°C

FIG. 10.49
741 op-amp specifications.

Electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = – 15 V

PARAMETER		TEST CONDITIONS †		uA741M MIN	uA741M TYP	uA741M MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	25°C		1	5	mV
			Full range			6	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0	25°C		± 15		mV
I_{IO}	Input offset current	V_O = 0	25°C		20	200	nA
			Full range			500	
I_{IB}	Input bias current	V_O = 0	25°C		80	500	nA
			Full range			1500	
V_{ICR}	Common-mode input voltage range		25°C	± 12	± 13		V
			Full range	± 12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	± 12	± 14		V
		R_L ≥ 10 kΩ	Full range	± 12			
		R_L = 2 kΩ	25°C	± 10	± 13		
		R_L ≥ 2 kΩ	Full range	± 10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ	25°C	50	200		V/mV
		V_O = ± 10 V	Full range	25			
r_i	Input resistance		25°C	0.3	2		MΩ
r_o	Output resistance	V_O = 0 See note 6	25°C		75		Ω
C_i	Input capacitance		25°C		1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	90		dB
			Full range	70			
k_{SVS}	Supply voltage sensitivity $\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ± 9 V to ± 15 V	25°C		30	150	μV/V
			Full range			150	
I_{OS}	Short-circuit output current		25°C		± 25	± 40	mA
I_{CC}	Supply current	No load, V_O = 0	25°C		1.7	2.8	mA
			Full range			3.3	
P_D	Total power dissipation	No load, V_O = 0	25°C		50	85	mW
			Full range			100	

Operating characteristics, V_{CC+} = 15 V, V_{CC-} = – 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	uA741M MIN	uA741M TYP	uA741M MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF		0.3		μs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF		0.5		V/μs

FIG. 10.49
Continued.

Absolute Maximum Ratings

The absolute maximum ratings provide information on what largest voltage supplies may be used, how large the input signal swing may be, and at how much power the device is capable of operating. Depending on the particular version of 741 used, the largest supply voltage is a dual supply of ±18 V or ±22 V. In addition, the IC can internally dissipate from 310 mW to 570 mW, depending on the IC package used. Table 10.2 summarizes some typical values to use in examples and problems.

TABLE 10.2
Absolute Maximum Ratings

Supply voltage	±22 V
Internal power dissipation	500 mW
Differential input voltage	±30 V
Input voltage	±15 V

EXAMPLE 10.15 Determine the current draw from a dual power supply of ±12 V if the IC dissipates 500 mW.

Solution: If we assume that each supply provides half the total power to the IC, then

$$P = VI$$

$$250 \text{ mW} = 12 \text{ V}(I)$$

so that each supply must provide a current of

$$I = \frac{250\text{ mW}}{12\text{ V}} = \mathbf{20.83\text{ mA}}$$

Electrical Characteristics

Electrical characteristics include many of the parameters covered earlier in this chapter. The manufacturer provides some combination of typical, minimum, or maximum values for various parameters as deemed most useful. A summary is provided in Table 10.3.

V_{IO} Input offset voltage: The input offset voltage is seen to be typically 1 mV, but can go as high as 6 mV. The output offset voltage is then computed based on the circuit used. If the worst condition possible is of interest, the maximum value should be used. Typical values are those more commonly expected when using the op-amp.

I_{IO} Input offset current: The input offset current is listed to be typically 20 nA, whereas the largest value expected is 200 nA.

I_{IB} Input bias current: The input bias current is typically 80 nA and may be as large as 500 nA.

V_{ICR} Common-mode input voltage range: This parameter lists the range over which the input voltage may vary (using a supply of ±15 V), about ±12 V to ±13 V. Inputs larger in amplitude than this value will probably result in output distortion and should be avoided.

V_{OM} Maximum peak output voltage swing: This parameter lists the largest amount the output may vary (using a ±15-V supply). Depending on the circuit closed-loop gain, the input signal should be limited to keep the output from varying by an amount no larger than ±12 V in the worst case, or by ±14 V typically.

A_{VD} Large-signal differential voltage amplification: This is the open-loop voltage gain of the op-amp. Although a minimum value of 20 V/mV, or 20,000 V/V is listed, the manufacturer also lists a typical value of 200 V/mV, or 200,000 V/V.

r_i Input resistance: The input resistance of the op-amp when measured under open-loop conditions is typically 2 MΩ, but could be as little as 0.3 MΩ or 300 kΩ. In a closed-loop circuit, this input impedance can be much larger, as discussed previously.

r_o Output resistance: The op-amp output resistance is listed as typically 75 Ω. No minimum or maximum value is given by the manufacturer for this op-amp. Again, in a closed-loop circuit, the output impedance can be lower, depending on the circuit gain.

TABLE 10.3

μA741 Electrical Characteristics: $V_{CC} = \pm 15$ V, $T_A = 25°C$

Characteristic	Minimum	Typical	Maximum	Unit
V_{IO} Input offset voltage		1	6	mV
I_{IO} Input offset current		20	200	nA
I_{IB} Input bias current		80	500	nA
V_{ICR} Common-mode input voltage range	±12	±13		V
V_{OM} Maximum peak output voltage swing	±12	±14		V
A_{VD} Large-signal differential voltage amplification	20	200		V/mV
r_i Input resistance	0.3	2		MΩ
r_o Output resistance		75		Ω
C_i Input capacitance		1.4		pF
CMRR Common-mode rejection ratio	70	90		dB
I_{CC} Supply current		1.7	2.8	mA
P_D Total power dissipation		50	85	mW

C_i Input capacitance: For high-frequency considerations, it is helpful to know that the input to the op-amp has typically 1.4 pF of capacitance, a generally small value compared even to stray wiring.

CMRR Common-mode rejection ratio: This parameter is seen to be typically 90 dB, but could go as low as 70 dB. Since 90 dB is equivalent to 31,622.78, the op-amp amplifies noise (common inputs) by over 30,000 times less than difference inputs.

I_{CC} Supply current: The op-amp draws a total of 2.8 mA, typically from the dual voltage supply, but the current drawn could be as little as 1.7 mA. This parameter helps the user determine the size of the voltage supply to use. It also can be used to calculate the power dissipated by the IC ($P_D = 2V_{CC}I_{CC}$).

P_D Total power dissipation: The total power dissipated by the op-amp is typically 50 mW but could go as high as 85 mW. Referring to the previous parameter, we see that the op-amp will dissipate about 50 mW when drawing about 1.7 mA using a dual 15-V supply. At smaller supply voltages, the current drawn will be less and the total power dissipated will also be less.

EXAMPLE 10.16 Using the specifications listed in Table 10.3, calculate the typical output offset voltage for the circuit connection of Fig. 10.50.

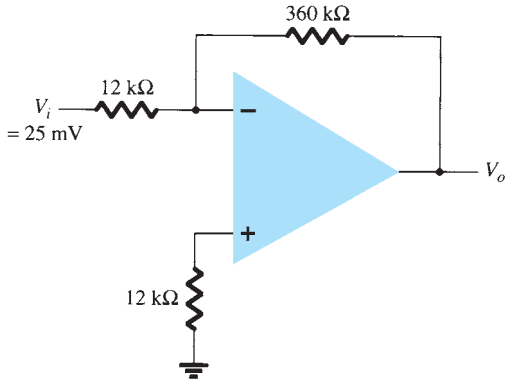


FIG. 10.50
Op-amp circuit for Examples 10.16, 10.17, and 10.19.

Solution: The output offset due to V_{IO} is calculated to be

$$\text{Eq. (10.16):} \quad V_o(\text{offset}) = V_{IO}\frac{R_1 + R_f}{R_1} = (1\text{ mV})\left(\frac{12\text{ k}\Omega + 360\text{ k}\Omega}{12\text{ k}\Omega}\right) = 31\text{ mV}$$

The output voltage due to I_{IO} is calculated to be

$$\text{Eq. (10.18):} \quad V_o(\text{offset}) = I_{IO}R_f = 20\text{ nA}\,(360\text{ k}\Omega) = 7.2\text{ mV}$$

Assuming that these two offsets are the same polarity at the output, we obtain for the total output offset voltage

$$V_o(\text{offset}) = 31\text{ mV} + 7.2\text{ mV} = \mathbf{38.2\text{ mV}}$$

EXAMPLE 10.17 For the typical characteristics of the 741 op-amp ($r_o = 75\ \Omega, A = 200\text{ k}\Omega$), calculate the following values for the circuit of Fig. 10.50:

a. A_{CL}.
b. Z_i.
c. Z_o.

Solution:

a. Eq. (10.8): $\dfrac{V_o}{V_i} = -\dfrac{R_f}{R_1} = -\dfrac{360\ \text{k}\Omega}{12\ \text{k}\Omega} = \mathbf{-30} \cong \dfrac{1}{\beta}$

b. $Z_i = R_1 = \mathbf{12\ k\Omega}$

c. $Z_o = \dfrac{r_o}{(1 + \beta A)} = \dfrac{75\ \Omega}{1 + \left(\dfrac{1}{30}\right)(200\ \text{k}\Omega)} = \mathbf{0.011\ \Omega}$

Operating Characteristics

Another group of values used to describe the operation of the op-amp over varying signals is provided in Table 10.4.

TABLE 10.4

Operating Characteristics: $V_{CC} = \pm 15$ V, $T_A = 25°C$

Parameter	Minimum	Typical	Maximum	Unit
B_1 Unity gain bandwidth		1		MHz
t_r Rise time		0.3		μs

EXAMPLE 10.18 Calculate the cutoff frequency of an op-amp having characteristics given in Tables 10.3 and 10.4.

Solution:

$$\text{Eq. (10.23):}\quad f_C = \frac{f_1}{A_{\text{VD}}} = \frac{B_1}{A_{\text{VD}}} = \frac{1\ \text{MHz}}{20{,}000} = \mathbf{50\ Hz}$$

EXAMPLE 10.19 Calculate the maximum frequency of the input signal for the circuit in Fig. 10.50 with an input of $V_i = 25$ mV.

Solution: For a closed-loop gain of $A_{\text{CL}} = 30$ and an input of $V_i = 25$ mV, the output gain factor is calculated to be

$$K = A_{\text{CL}}V_i = 30(25\ \text{mV}) = 750\ \text{mV} = 0.750\ \text{V}$$

Using Eq. (10.25), we obtain the maximum signal frequency $f_{\max}$ as

$$f_{\max} = \frac{\text{SR}}{2\pi K} = \frac{0.5\ \text{V}/\mu\text{s}}{2\pi(0.750\ \text{V})} = \mathbf{106\ kHz}$$

Op-Amp Performance

The manufacturer provides a number of graphical descriptions to describe the performance of the op-amp. Figure 10.51 includes some typical performance curves comparing various characteristics as a function of supply voltage. The open-loop voltage gain is seen to get larger with a larger supply voltage value. Whereas the previous tabular information provided information at a particular supply voltage, the performance curve shows how the voltage gain is affected by using a range of supply voltage values.

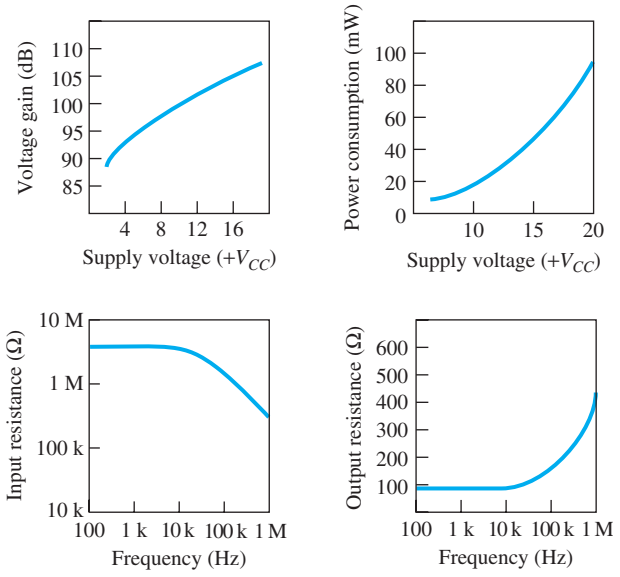


FIG. 10.51
Performance curves.

EXAMPLE 10.20 Using Fig. 10.51, determine the open-loop voltage gain for a supply voltage of $V_{CC} = \pm 12$ V.

Solution: From the curve in Fig. 10.51, $A_{VD} \approx 104$ dB. This is a linear voltage gain of

$$A_{VD}(\text{dB}) = 20 \log_{10} A_{VD}$$
$$104 \text{ dB} = 20 \log A_{VD}$$
$$A_{VD} = \text{antilog} \frac{104}{20} = \mathbf{158.5 \times 10^3}$$

Another performance curve in Fig. 10.51 shows how power consumption varies as a function of supply voltage. As shown, the power consumption increases with larger values of supply voltage. For example, whereas the power dissipation is about 50 mW at $V_{CC} = \pm 15$ V, it drops to about 5 mW with $V_{CC} = \pm 5$ V. Two other curves show how the input and output resistances are affected by frequency: The input impedance drops and the output resistance increases at higher frequency.

10.9 DIFFERENTIAL AND COMMON-MODE OPERATION

One of the more important features of a differential circuit connection, as provided in an op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs while only slightly amplifying signals that are common to both inputs. An op-amp provides an output component that is due to the amplification of the difference of the signals applied to the plus and minus inputs and a component due to the signals common to both inputs. Since amplification of the opposite input signals is much greater than that of the common input signals, the circuit provides a common-mode rejection as described by a numerical value called the common-mode rejection ratio (CMRR).

Differential Inputs

When separate inputs are applied to the op-amp, the resulting difference signal is the difference between the two inputs.

$$V_d = V_{i_1} - V_{i_2} \qquad \textbf{(10.26)}$$

Common Inputs

When both input signals are the same, a common signal element due to the two inputs can be defined as the average of the sum of the two signals.

$$V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) \tag{10.27}$$

Output Voltage

Since any signals applied to an op-amp in general have both in-phase and out-of-phase components, the resulting output can be expressed as

$$V_o = A_d V_d + A_c V_c \tag{10.28}$$

where V_d = difference voltage given by Eq. (10.26)
V_c = common voltage given by Eq. (10.27)
A_d = differential gain of the amplifier
A_c = common-mode gain of the amplifier

Opposite-Polarity Inputs

If opposite-polarity inputs applied to an op-amp are ideally opposite signals, $V_{i_1} = -V_{i_2} = V_s$, the resulting difference voltage is

$$\text{Eq. (10.26):} \quad V_d = V_{i_1} - V_{i_2} = V_s - (-V_s) = 2V_s$$

and the resulting common voltage is

$$\text{Eq. (10.27):} \quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}[V_s + (-V_s)] = 0$$

so that the resulting output voltage is

$$\text{Eq. (10.28):} \quad V_o = A_d V_d + A_c V_c = A_d(2V_s) + 0 = 2A_d V_s$$

This shows that when the inputs are an ideal opposite signal (no common element), the output is the differential gain times twice the input signal applied to one of the inputs.

Same-Polarity Inputs

If the same-polarity inputs are applied to an op-amp, $V_{i_1} = V_{i_2} = V_s$, the resulting difference voltage is

$$\text{Eq. (10.26):} \quad V_d = V_{i_1} - V_{i_2} = V_s - V_s = 0$$

and the resulting common voltage is

$$\text{Eq. (10.27):} \quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}(V_s + V_s) = V_s$$

so that the resulting output voltage is

$$\text{Eq. (10.28):} \quad V_o = A_d V_d + A_c V_c = A_d(0) + A_c V_s = A_c V_s$$

This shows that when the inputs are ideal in-phase signals (no difference signal), the output is the common-mode gain times the input signal V_s, which shows that only common-mode operation occurs.

Common-Mode Rejection

The solutions above provide the relationships that can be used to measure A_d and A_c in op-amp circuits.

1. *To measure* A_d: Set $V_{i_1} = -V_{i_2} = V_s = 0.5$ V, so that

$$\text{Eq. (10.26):} \quad V_d = (V_{i_1} - V_{i_2}) = (0.5\text{ V} - (-0.5\text{ V}) = 1\text{ V}$$

and

$$\text{Eq. (10.27):} \quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}[0.5\text{ V} + (-0.5\text{ V})] = 0\text{ V}$$

Under these conditions the output voltage is

$$\text{Eq. (10.28):} \quad V_o = A_d V_d + A_c V_c = A_d(1\text{ V}) + A_c(0) = A_d$$

Thus, setting the input voltages $V_{i_1} = -V_{i_2} = 0.5$ V results in an output voltage numerically equal to the value of A_d.

2. *To measure* A_c: Set $V_{i_1} = V_{i_2} = V_s = 1$ V, so that

$$\text{Eq. (10.26):} \quad V_d = (V_{i_1} - V_{i_2}) = (1\text{ V} - 1\text{ V}) = 0\text{ V}$$

and

$$\text{Eq. (10.27):} \quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}(1\text{ V} + 1\text{ V}) = 1\text{ V}$$

Under these conditions the output voltage is

$$\text{Eq. (10.28):} \quad V_o = A_d V_d + A_c V_c = A_d(0\text{ V}) + A_c(1\text{ V}) = A_c$$

Thus, setting the input voltages $V_{i_1} = V_{i_2} = 1$ V results in an output voltage numerically equal to the value of A_c.

Common-Mode Rejection Ratio

Having obtained A_d and A_c (as in the measurement procedure discussed above), we can now calculate a value for the common-mode rejection ratio (CMRR), which is defined by the following equation:

$$\boxed{\text{CMRR} = \frac{A_d}{A_c}} \tag{10.29}$$

The value of CMRR can also be expressed in logarithmic terms as

$$\boxed{\text{CMRR (log)} = 20\log_{10}\frac{A_d}{A_c}\ \text{(dB)}} \tag{10.30}$$

EXAMPLE 10.21 Calculate the CMRR for the circuit measurements shown in Fig. 10.52.

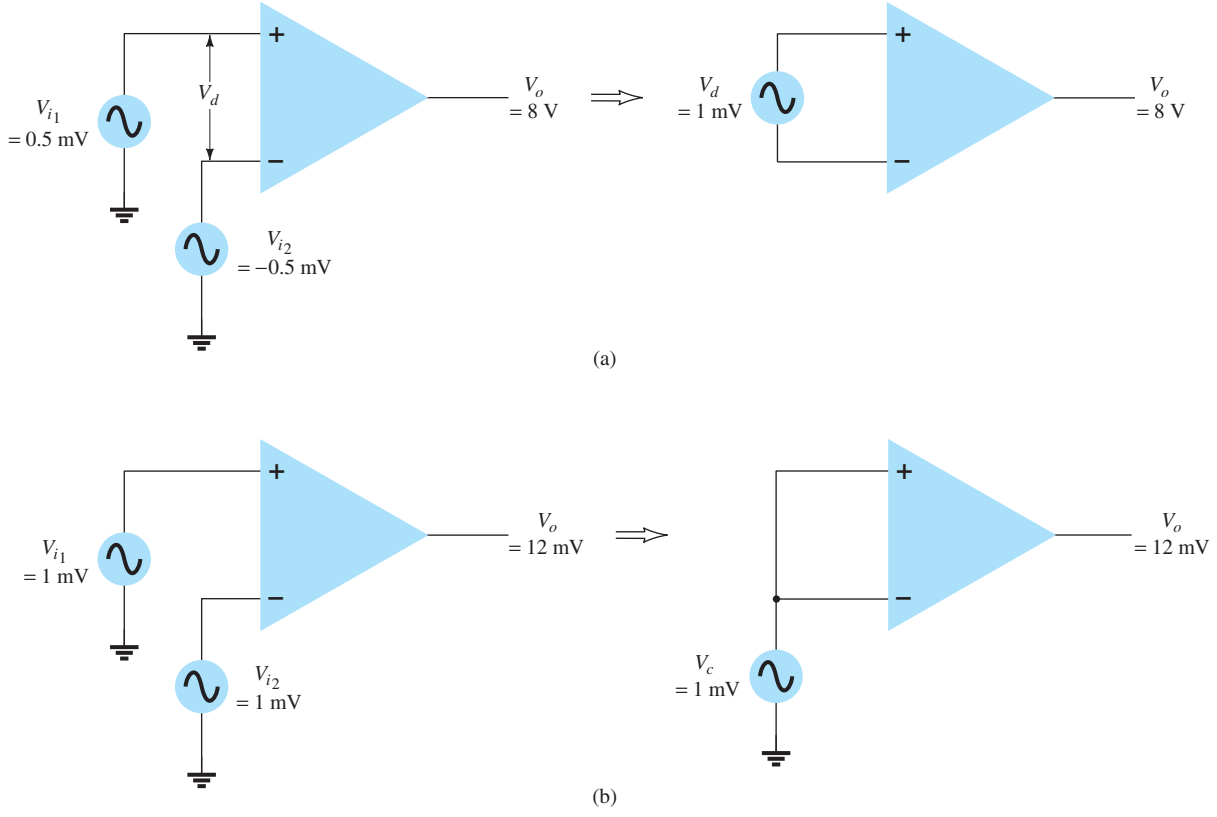


FIG. 10.52
(a) Differential and (b) common-mode operation.

Solution: From the measurement shown in Fig. 10.52a, using the procedure in step 1 above, we obtain

$$A_d = \frac{V_o}{V_d} = \frac{8\text{ V}}{1\text{ mV}} = 8000$$

The measurement shown in Fig. 10.52b, using the procedure in step 2 above, gives us

$$A_c = \frac{V_o}{V_c} = \frac{12\text{ mV}}{1\text{ mV}} = 12$$

Using Eq. (10.28), we obtain the value of CMRR,

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{8000}{12} = \mathbf{666.7}$$

which can also be expressed as

$$\text{CMRR} = 20\log_{10}\frac{A_d}{A_c} = 20\log_{10} 666.7 = \mathbf{56.48\text{ dB}}$$

It should be clear that the desired operation will have A_d very large with A_c very small. That is, the signal components of opposite polarity will appear greatly amplified at the output, whereas the signal components that are in phase will mostly cancel out so that the common-mode gain A_c is very small. Ideally, the value of the CMRR is infinite. Practically, the larger the value of CMRR, the better is the circuit operation.

We can express the output voltage in terms of the value of CMRR as follows:

$$\text{Eq. (12.22):}\quad V_o = A_dV_d + A_cV_c = A_dV_d\left(1 + \frac{A_cV_c}{A_dV_d}\right)$$

Using Eq. (12.24), we can write the above as

$$\boxed{V_o = A_dV_d\left(1 + \frac{1}{\text{CMRR}}\frac{V_c}{V_d}\right)} \qquad \textbf{(10.31)}$$

Even when both V_d and V_c components of a signal are present, Eq. (10.31) shows that for large values of CMRR, the output voltage will be due mostly to the difference signal, with the common-mode component greatly reduced or rejected. Some practical examples should help clarify this idea.

EXAMPLE 10.22 Determine the output voltage of an op-amp for input voltages of $V_{i_1} = 150\ \mu\text{V}$ and $V_{i_2} = 140\ \mu\text{V}$. The amplifier has a differential gain of $A_d = 4000$ and the value of CMRR is:

a. 100.
b. 10^5.

Solution:

$$\text{Eq. (10.26):}\quad V_d = V_{i_1} - V_{i_2} = (150 - 140)\,\mu\text{V} = 10\,\mu\text{V}$$

$$\text{Eq. (10.27):}\quad V_c = \frac{1}{2}(V_{i_1} + V_{i_2}) = \frac{150\,\mu\text{V} + 140\,\mu\text{V}}{2} = 145\,\mu\text{V}$$

a.
$$\text{Eq. (10.31):}\quad V_o = A_dV_d\left(1 + \frac{1}{\text{CMRR}}\frac{V_c}{V_d}\right)$$

$$= (4000)(10\,\mu\text{V})\left(1 + \frac{1}{100}\frac{145\,\mu\text{V}}{10\,\mu\text{V}}\right)$$

$$= 40\text{ mV}(1.145) = \mathbf{45.8\text{ mV}}$$

b. $$V_o = (4000)(10\,\mu\text{V})\left(1 + \frac{1}{10^5}\frac{145\,\mu\text{V}}{10\,\mu\text{V}}\right) = 40\text{ mV}(1.000145) = \mathbf{40.006\text{ mV}}$$

Example 10.22 shows that the larger the value of CMRR, the closer is the output voltage to the difference input times the difference gain with the common-mode signal being rejected.

10.10 SUMMARY

Important Conclusions and Concepts

1. Differential operation involves the use of opposite-polarity inputs.
2. Common-mode operation involves the use of the same-polarity inputs.
3. Common-mode rejection compares the gain for differential inputs to that for common inputs.
4. An op-amp is an **op**erational **amp**lifier.
5. The basic features of an op-amp are:
   Very high input impedance (typically megohms)
   Very high voltage gain (typically a few hundred thousand and greater)
   Low output impedance (typically less than 100 Ω)
6. Virtual ground is a concept based on the practical fact that the differential input voltage between plus (+) and minus (−) inputs is nearly (virtually) 0 V—when calculated as the output voltage (at most, that of the voltage supply) divided by the very high voltage gain of the op-amp.
7. Basic op-amp connections include:
   Inverting amplifier
   Noninverting amplifier
   Unity-gain amplifier
   Summing amplifier
   Integrator amplifier
8. Op-amp specs include:
   Offset voltages and currents
   Frequency parameters
   Gain–bandwidth
   Slew rate

Equations

$$\text{CMRR} = 20 \log_{10} \frac{A_d}{A_c}$$

Inverting amplifier:

$$\frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Noninverting amplifier:

$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

Unity follower:

$$V_o = V_1$$

Summing amplifier:

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$$

Integrator amplifier:

$$v_o(t) = -\frac{1}{RC} \int v_1(t)\, dt$$

$$\text{Slew rate (SR)} = \frac{\Delta V_o}{\Delta t} \qquad \text{V}/\mu\text{s}$$

10.11 COMPUTER ANALYSIS

PSpice Windows

Program 10.1—Inverting Op-Amp An inverting op-amp, shown in Fig. 10.53, is considered first. With the dc voltage display turned on, the result after running an analysis shows that for an input of 2 V and a circuit gain of −5,

$$A_v = -R_F/R_1 = -500\,\text{k}\Omega/100\,\text{k}\Omega = -5$$

The output is exactly −10 V:

$$V_o = A_v V_i = -5(2\text{ V}) = -10\text{ V}$$

The input to the minus terminal is −50.01 μV, which is virtually ground, or 0 V.

A practical inverting op-amp circuit is drawn in Fig. 10.54. Using the same resistor values as in Fig. 10.53 with a practical op-amp unit, the μA741, we obtain the resulting output of −9.96 V, near the ideal value of −10 V. This slight difference from the ideal is due to the actual gain and input impedance of the μA741 op-amp unit.

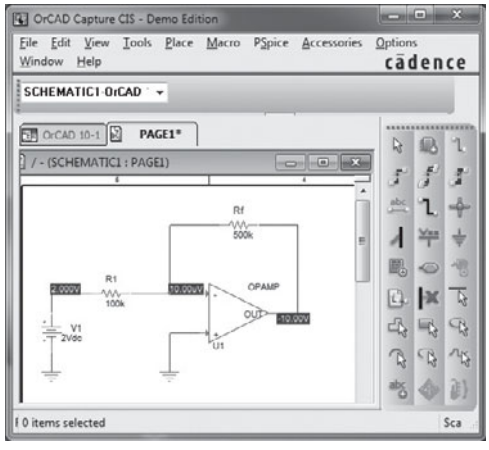


FIG. 10.53
Inverting op-amp using ideal model.

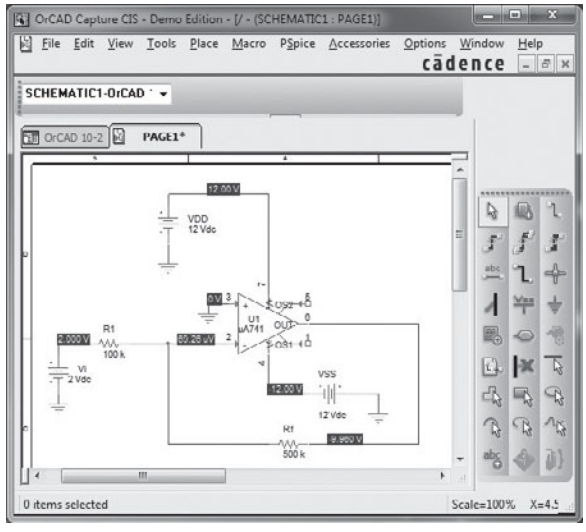


FIG. 10.54
Practical inverting op-amp circuit.

Before the analysis is done, selecting **Analysis Setup, Transfer Function,** and then **Output** of **V(RF:2)** and **Input Source** of V_i will provide the small-signal characteristics in the output listing. The circuit gain is seen to be

$$V_o/V_i = -5$$

Input resistance at $V_i = 1 \times 10^5$

Output resistance at $V_o = 4.95 \times 10^{-3}$

Program 10.2—Noninverting Op-Amp Figure 10.55 shows a noninverting op-amp circuit. The bias voltages are displayed on the figure. The theoretical gain of the amplifier circuit should be

$$A_v = (1 + R_F/R_1) = 1 + 500\,\text{k}\Omega/100\,\text{k}\Omega = 6$$

For an input of 2 V, the resulting output will be

$$V_o = A_v V_i = 5(2\text{ V}) = 10\text{ V}$$

The output is noninverted from the input.

Program 10.3—Summing Op-Amp Circuit A summing op-amp circuit such as that in Example 10.3 is shown in Fig. 10.56. Bias voltages also are displayed in Fig. 10.56, showing the resulting output at 3 V, as was calculated in Example 10.3. Notice how well the virtual ground concept works with the minus input being only 3.791 μV.

Program 10.4—Unity-Gain Op-Amp Circuit Figure 10.57 shows a unity-gain op-amp circuit with bias voltages displayed. For an input of +2 V, the output is exactly +2 V.

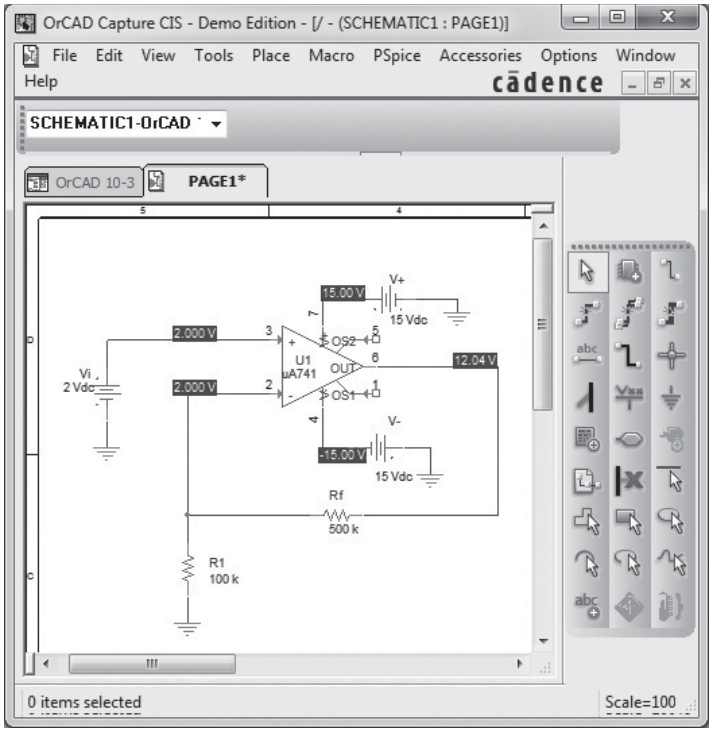


FIG. 10.55
Design Center schematic for noninverting op-amp circuit.

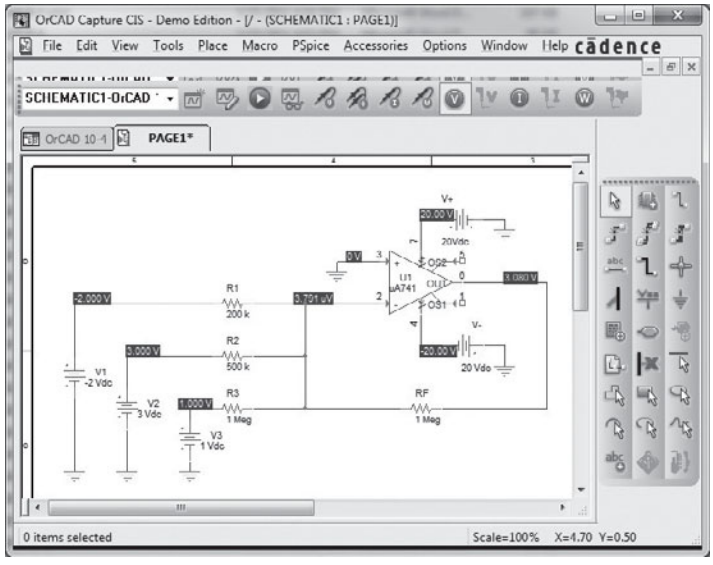


FIG. 10.56
Summing amplifier for Program 10.3.

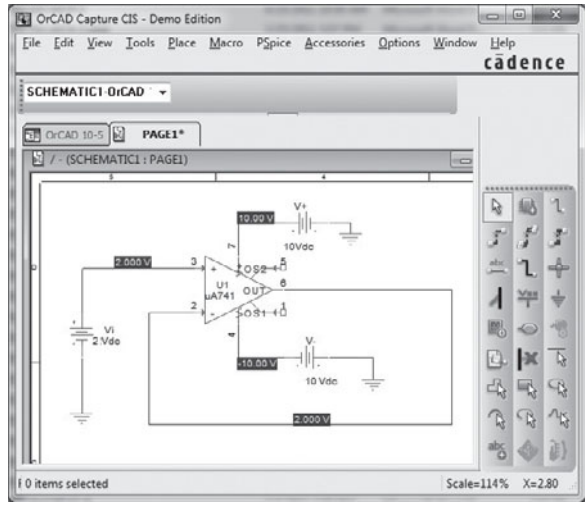


FIG. 10.57
Unity-gain amplifier.

Program 10.5—Op-Amp Integrator Circuit An op-amp integrator circuit is shown in Fig. 10.58. The input is selected as **VPULSE,** which is set to be a step input as follows: Set **ac** = 0, **dc** = 0, **V1** = 0 V, **V2** = 2 V, **TD** = 0, **TR** = 0, **TF** = 0, **PW** = 10 ms, and **PER** = 20 ms. This provides a step from 0 to 2 V, with no time delay, rise time, or fall time, having a period of 10 ms and repeating after a period of 20 ms. For this problem, the voltage rises instantly to 2 V, then stays there for a sufficiently long time for the output to drop as a ramp voltage from the maximum supply level of +20 V to the lowest level of −20 V. Theoretically, the output for the circuit of Fig. 10.58 is

$$v_o(t) = -1/RC \int v_i(t)\, dt$$

$$v_o(t) = -1/(10\,\text{k}\Omega)(0.01\,\mu\text{F}) \int 2\, dt = -10{,}000 \int 2\, dt = -20{,}000t$$

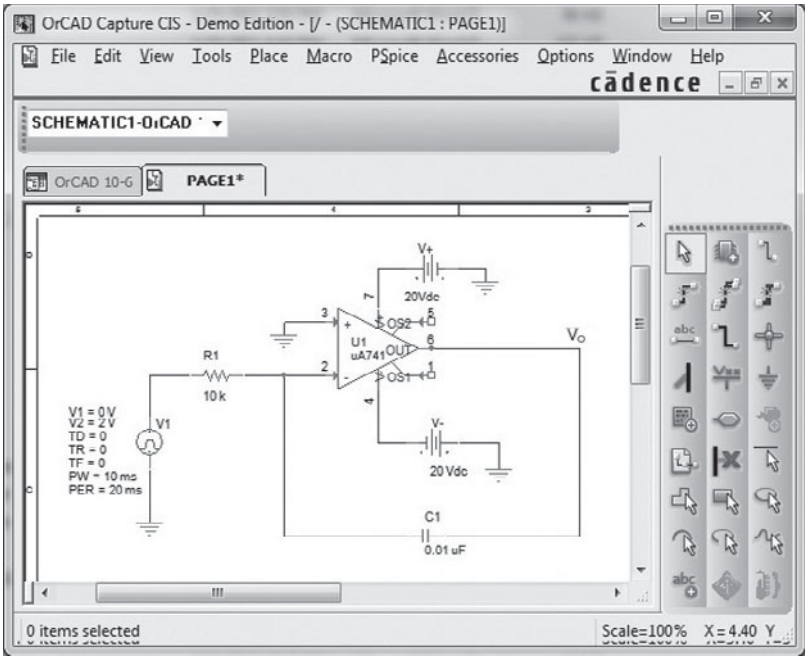


FIG. 10.58
Op-amp integrator circuit.

This is a negative ramp voltage dropping at a rate (slope) of −20,000 V/s. This ramp voltage will drop from +20 V to −20 V in

$$40\ \text{V}/20{,}000 = 2 \times 10^{-3} = 2\ \text{ms}$$

Figure 10.59 shows the input step waveform and the resulting output ramp waveform obtained using **PROBE.**

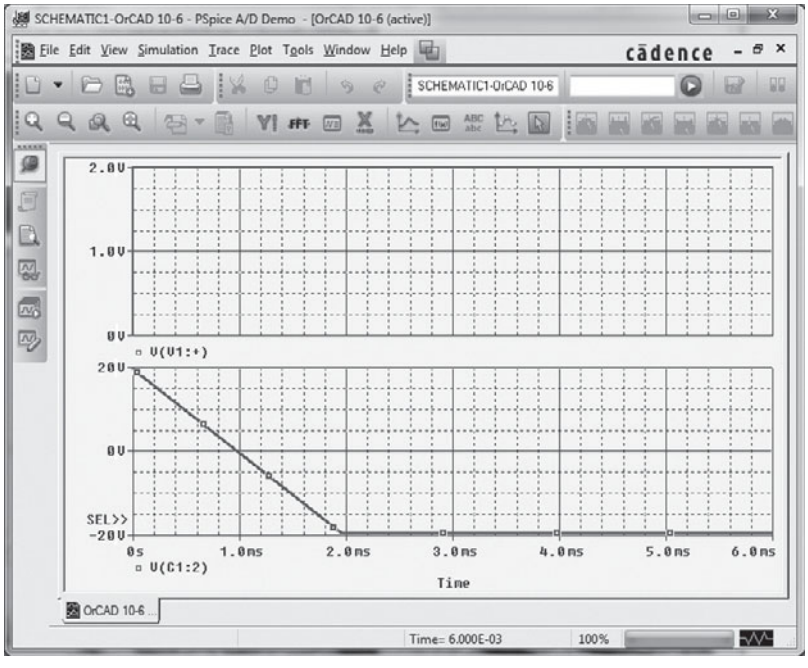
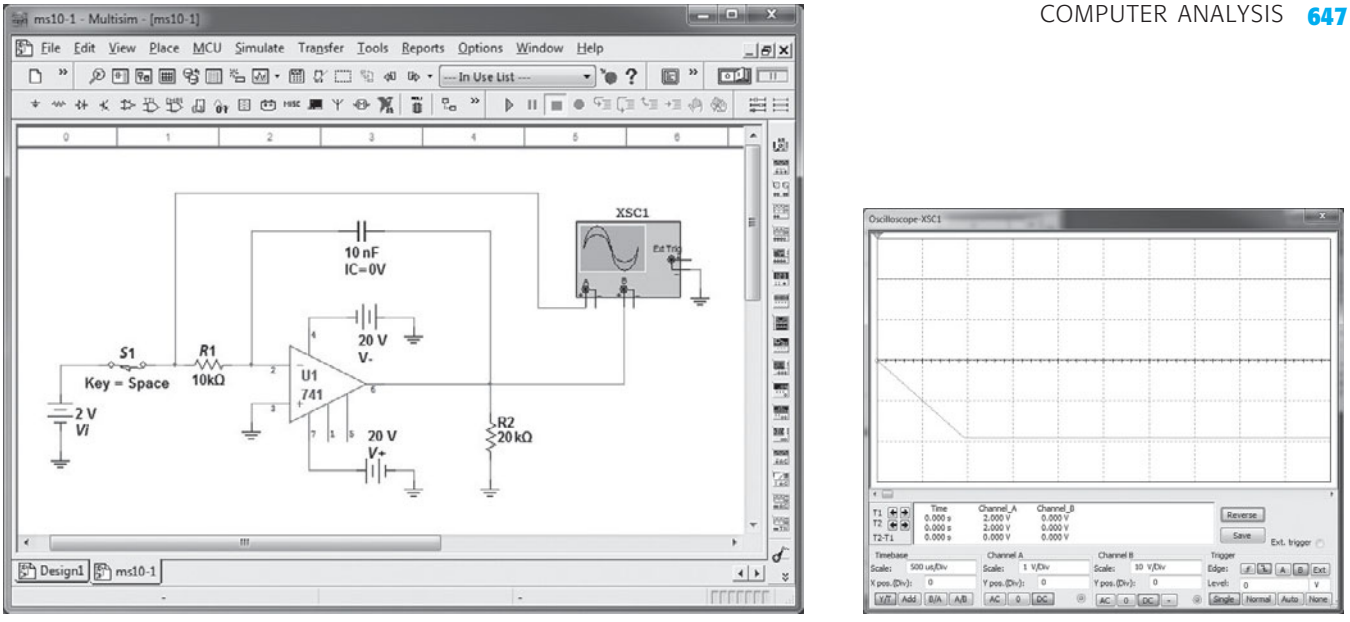


FIG. 10.59
Probe waveform for integrator circuit.

Multisim

The same integrator circuit can be constructed and operated using Multisim. Figure 10.60a shows the integrator circuit built using Multisim, with an oscilloscope connected to the



(a) (b)

FIG. 10.60

Multisim integrator circuit: (a) circuit; (b) waveform.

op-amp output. The oscilloscope graph obtained is shown in Fig. 10.60b, the linear output waveform going from +20 V down to −20 V in a period of about 2 ms.

Program 10.6–Multistage Op-Amp Circuit A multistage op-amp circuit is shown in Fig. 10.61. The input to stage 1 of 200 mV provides an output of 200 mV to stages 2 and 3. Stage 2 is an inverting amplifier with gain $-200\ \text{k}\Omega/20\ \text{k}\Omega = -10$, with an output from stage 2 of $-10(200\ \text{mV}) = -2$ V. Stage 3 is a noninverting amplifier with gain of $(1 + 200\ \text{k}\Omega/10\ \text{k}\Omega = 21)$, resulting in an output of $21(200\ \text{mV}) = 4.2$ V.

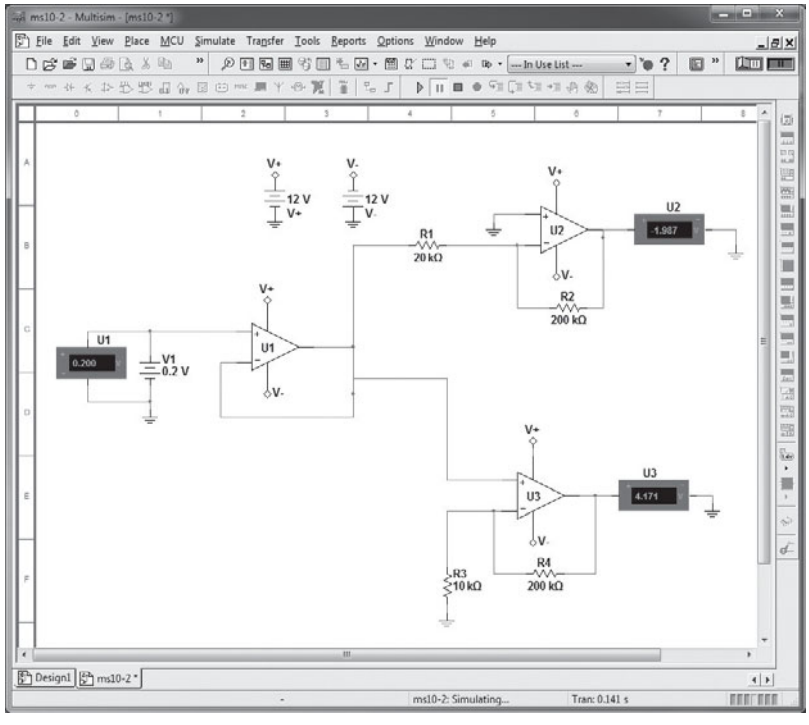


FIG. 10.61

Multistage op-amp circuit.

PROBLEMS

Note: Asterisks indicate more difficult problems.

10.5 Practical Op-Amp Circuits

1. What is the output voltage in the circuit of Fig. 10.62?

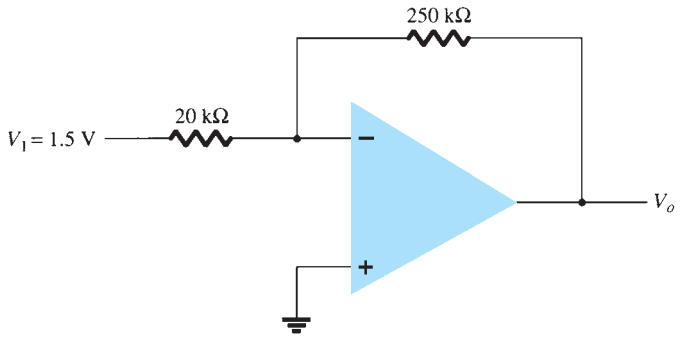


FIG. 10.62
Problems 1 and 25.

2. What is the range of the voltage-gain adjustment in the circuit of Fig. 10.63?

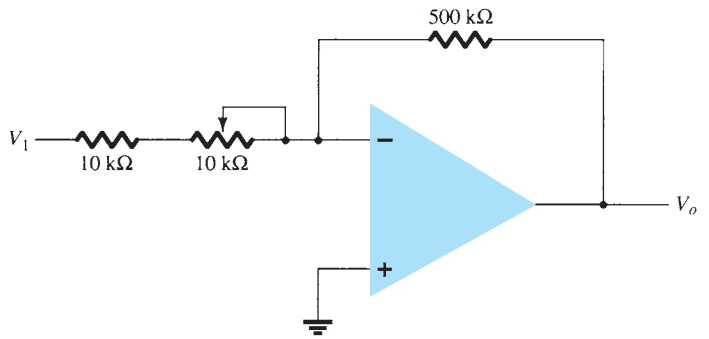


FIG. 10.63
Problem 2.

3. What input voltage results in an output of 2 V in the circuit of Fig. 10.64?

4. What is the range of the output voltage in the circuit of Fig. 10.65 if the input can vary from 0.1 to 0.5 V?

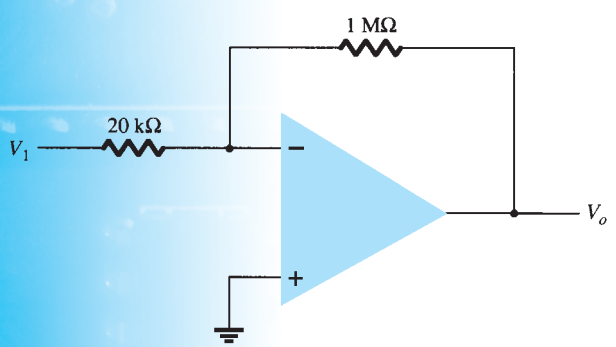


FIG. 10.64
Problem 3.

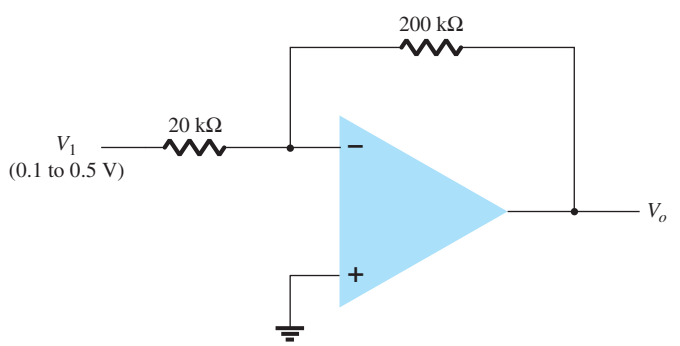


FIG. 10.65
Problem 4.

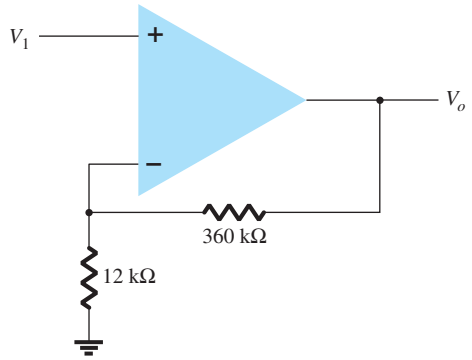


FIG. 10.66
Problems 5, 6, and 26.

5. What output voltage results in the circuit of Fig. 10.66 for an input of $V_1 = -0.3$ V?

6. What input must be applied to the input of Fig. 10.66 to result in an output of 2.4 V?

7. What range of output voltage is developed in the circuit of Fig. 10.67?

8. Calculate the output voltage developed by the circuit of Fig. 10.68 for $R_f = 330\ \text{k}\Omega$.

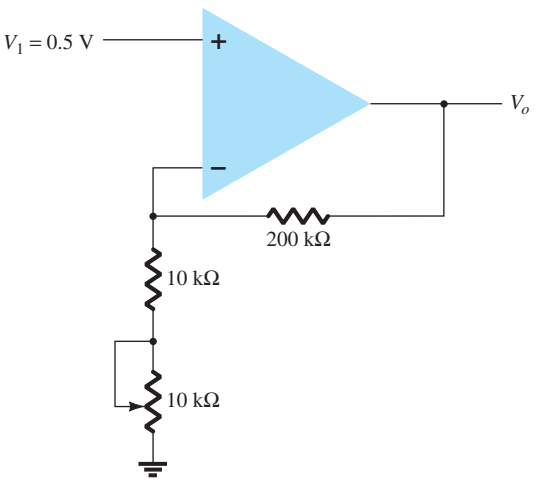


FIG. 10.67
Problem 7.

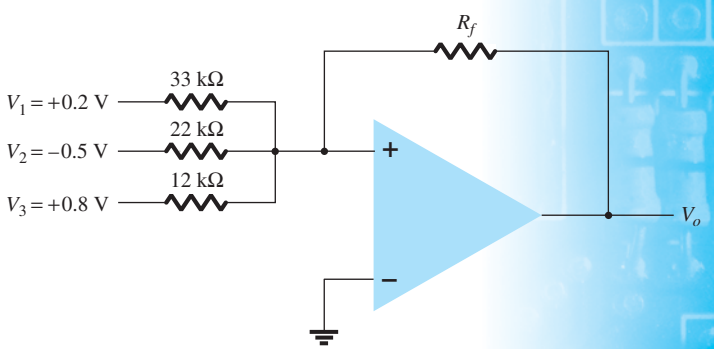


FIG. 10.68
Problems 8, 9, and 27.

9. Calculate the output voltage of the circuit in Fig. 10.68 for $R_f = 68\ \text{k}\Omega$.

10. Sketch the output waveform resulting in Fig. 10.69.

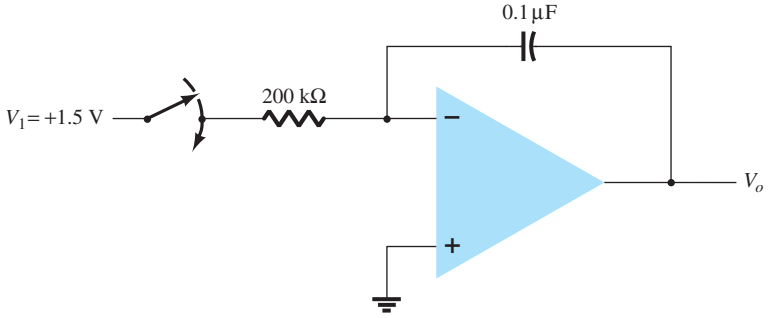


FIG. 10.69
Problem 10.

11. What output voltage results in the circuit of Fig. 10.70 for $V_1 = +0.5$ V?

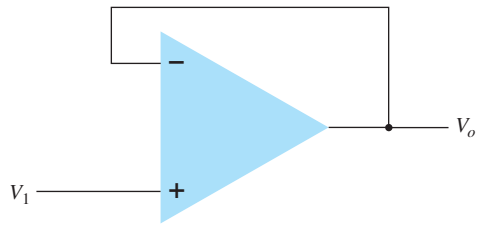


FIG. 10.70
Problem 11.

12. Calculate the output voltage for the circuit of Fig. 10.71.

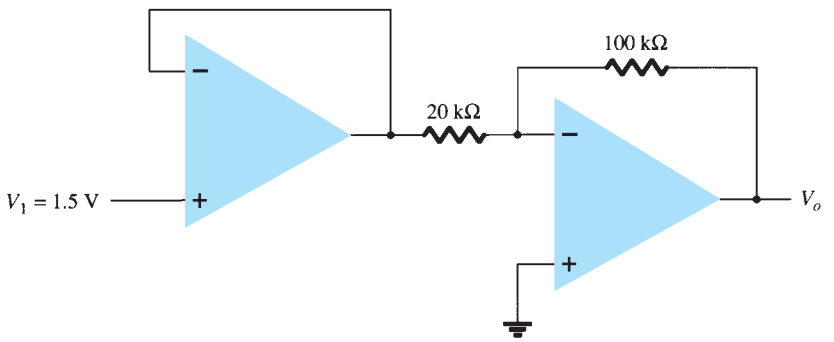


FIG. 10.71
Problems 12 and 28.

13. Calculate the output voltages V_2 and V_3 in the circuit of Fig. 10.72.

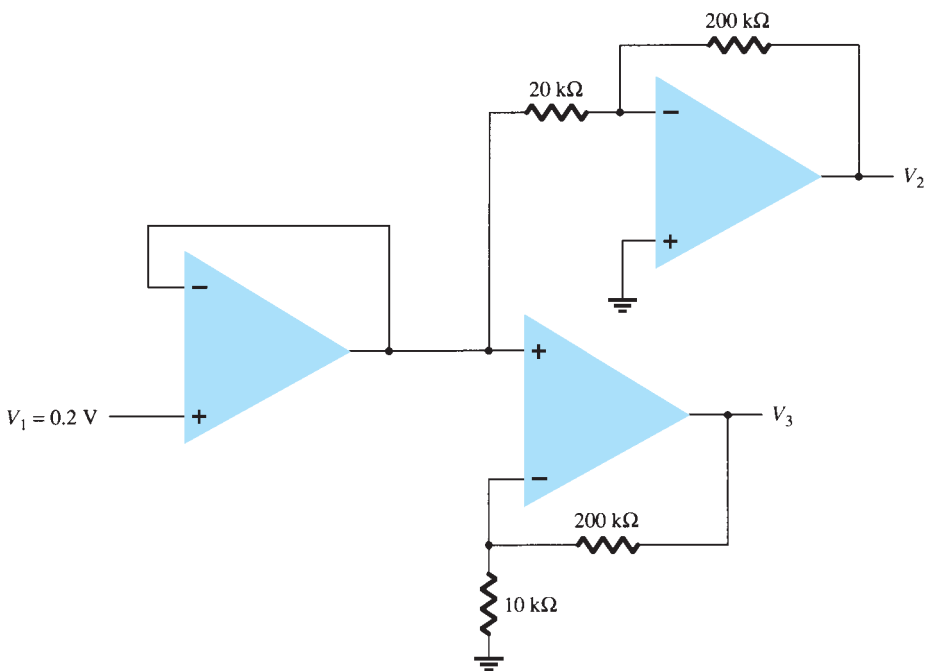


FIG. 10.72
Problem 13.

14. Calculate the output voltage, V_o, in the circuit of Fig. 10.73.

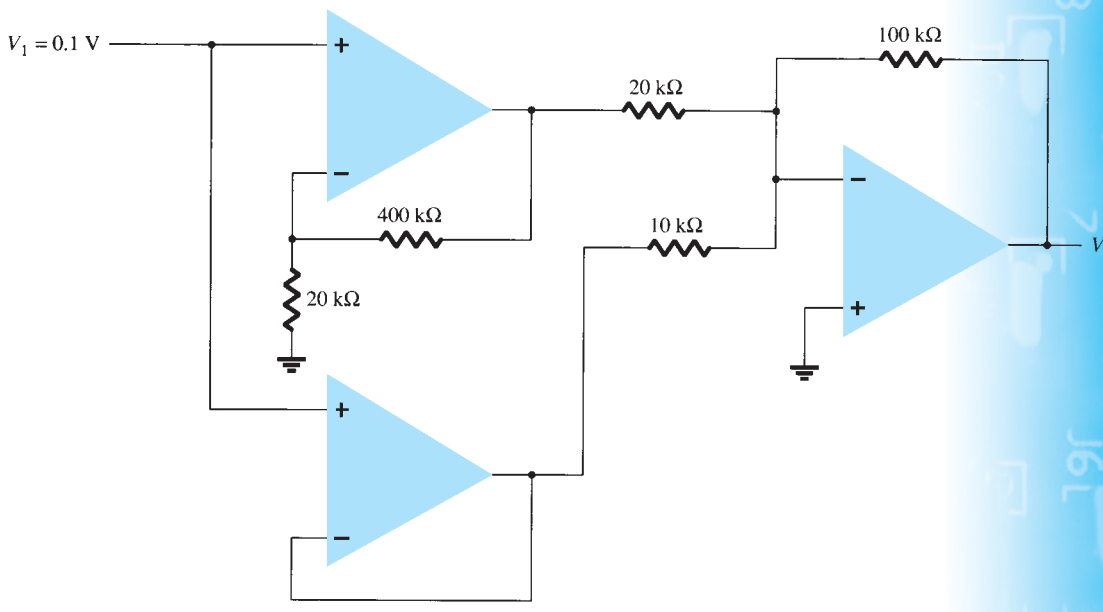


FIG. 10.73
Problems 14 and 29.

15. Calculate V_o in the circuit of Fig. 10.74.

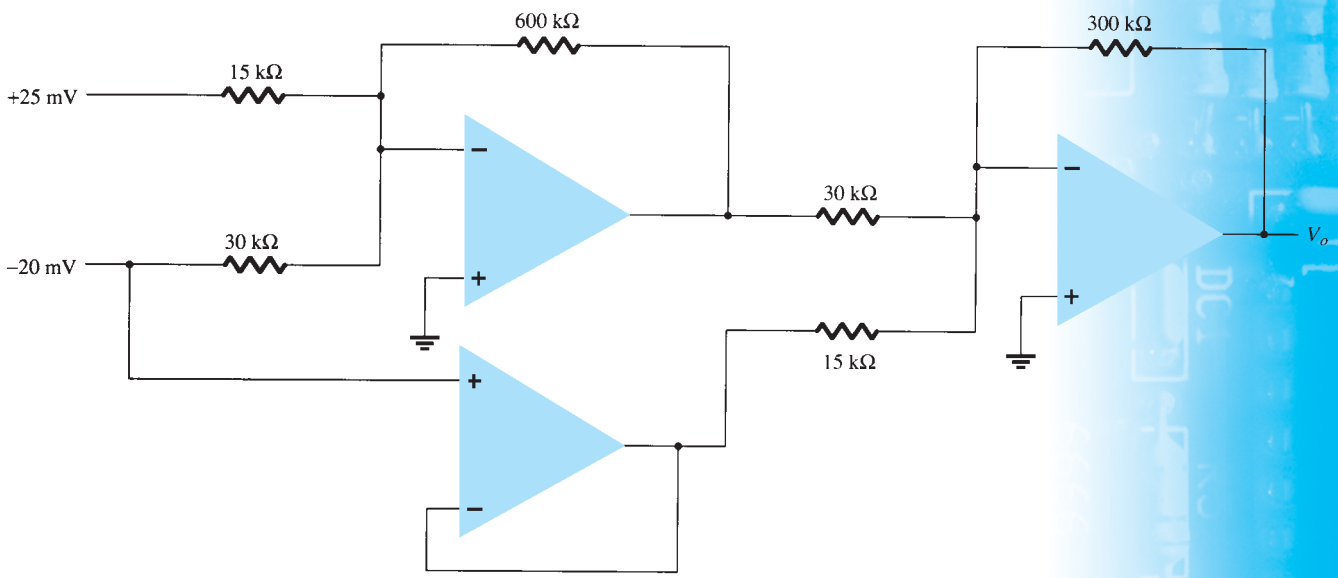


FIG. 10.74
Problems 15 and 30.

10.6 Op-Amp Specifications—DC Offset Parameters

***16.** Calculate the total offset voltage for the circuit of Fig. 10.75 for an op-amp with specified values of input offset voltage $V_{IO} = 6$ mV and input offset current $I_{IO} = 120$ nA.

***17.** Calculate the input bias current at each input of an op-amp having specified values of $I_{IO} = 4$ nA and $I_{IB} = 20$ nA.

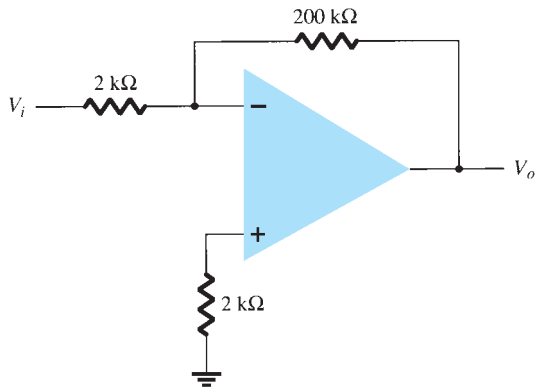


FIG. 10.75
Problems 16, 20, 21, and 22.

10.7 Op-Amp Specifications—Frequency Parameters

18. Determine the cutoff frequency of an op-amp having specified values $B_1 = 800\,\text{kHz}$ and $A_{VD} = 150\,\text{V/mV}$.

***19.** For an op-amp having a slew rate of $\text{SR} = 2.4\,\text{V}/\mu\text{s}$, what is the maximum closed-loop voltage gain that can be used when the input signal varies by 0.3 V in 10 μs?

***20.** For an input of $V_1 = 50\,\text{mV}$ in the circuit of Fig. 10.75, determine the maximum frequency that may be used. The op-amp slew rate $\text{SR} = 0.4\,\text{V}/\mu\text{s}$.

***21.** Using the specifications listed in Table 10.3, calculate the typical offset voltage for the circuit connection of Fig. 10.75.

***22.** For the typical characteristics of the 741 op-amp, calculate the following values for the circuit of Fig. 10.75:

a. A_{CL}.
b. Z_i.
c. Z_o.

10.9 Differential and Common-Mode Operation

23. Calculate the CMRR (in dB) for the circuit measurements of $V_d = 1\,\text{mV}$, $V_o = 120\,\text{mV}$, $V_C = 1\,\text{mV}$, and $V_o = 20\,\mu\text{V}$.

24. Determine the output voltage of an op-amp for input voltages of $V_{i_1} = 200\,\mu\text{V}$ and $V_{i_2} = 140\,\mu\text{V}$. The amplifier has a differential gain of $A_d = 6000$ and the value of CMRR is:

a. 200.
b. 10^5.

10.11 Computer Analysis

***25.** Use Schematic Capture or Multisim to draw a circuit to determine the output voltage in the circuit of Fig. 10.62.

***26.** Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.66 for the input of $V_i = 0.5\,\text{V}$.

***27.** Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.68 for $R_f = 68\,\text{k}\Omega$.

***28.** Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.71.

***29.** Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.73.

***30.** Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.74.

***31.** Use Schematic Capture or Multisim to obtain the output waveform for a 2-V step input to an integrator circuit, as shown in Fig. 10.39 with values of $R = 40\,\text{k}\Omega$ and $C = 0.003\,\mu\text{F}$.