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| MULTILEVEL INVERTER | عنوان المحاضرة باللغة الإنجليزية |
| العاكس متعدد المستويات | عنوان المحاضرة باللغة العربية |
| 6 | رقم المحاضرة |
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MULTILEVEL INVERTER

The multilevel inverter (MLI) is recently applied in many industrial applications, such converter has some advantages, such that has the ability to reduce the voltage stress on each power device due to utilization of multiple level on the dc bus, and harmonic reduction in the output voltage waveform even at low frequency, high voltage on DC side can be used. The multilevel starts from three levels and up, as the number of levels reaches to infinity, the output THD approaches to zero. The number of level is limited by voltage unbalance problem, voltage clamping requirements, and packaging constrain. There are three main MLI circuit topologies:

- 1) Diode- clamped multilevel inverter (DCMI) .
- 2) Flying-capacitor multilevel inverter (FCMI) .
- 3) Cascaded multilevel inverter with separate DC source .

1 Diode clamped multilevel inverter (DCMI)

The diode clamped multilevel inverter consists of series capacitors that divide the dc bus voltage into a set of capacitor voltages, to produce m-level output phase voltage, a (m-1) capacitors are required in the dc bus. The voltage across each capacitor is $V_{dc} / (m-1)$, the numbers of power device in the ON state are equal to (m-1). A single phase five level DCMI is shown in Fig. (5), the dc bus consists of four capacitors, the voltage on each capacitor is $(V_{dc}/4)$, on each device the voltage stress limited to one capacitor voltage.

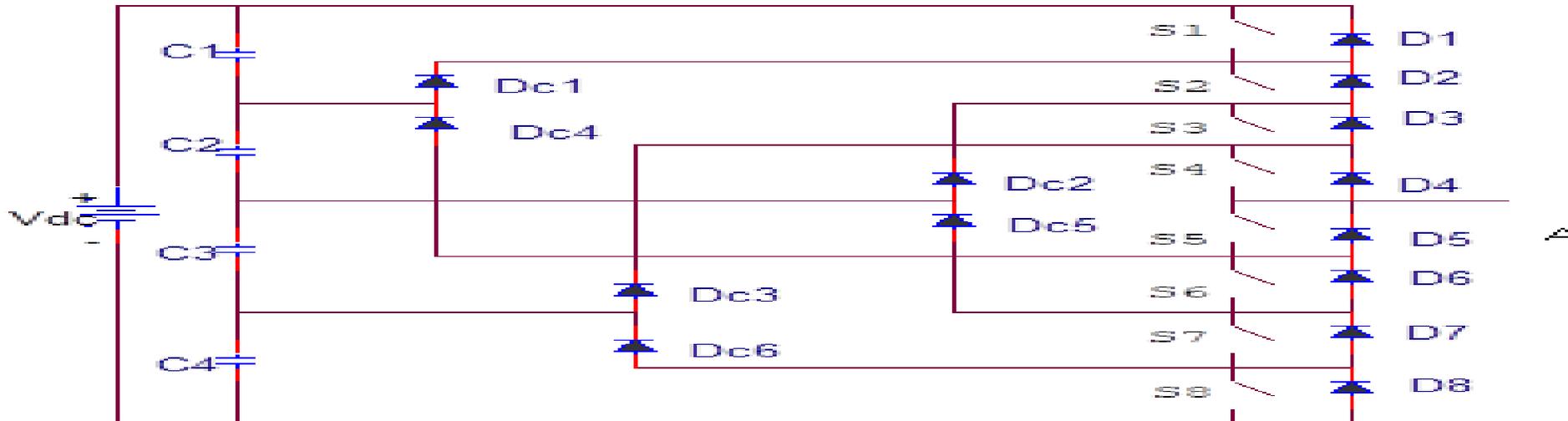


Fig. (5) five level single phase DCMI

2- Flying capacitor multilevel inverter (FCMI)

A FCMI shown in Fig. (6) employs separate capacitor precharged, the size of voltage increment between two capacitors defines the size of voltage step in out put voltage waveform, assuming each capacitor used has the same voltage rating

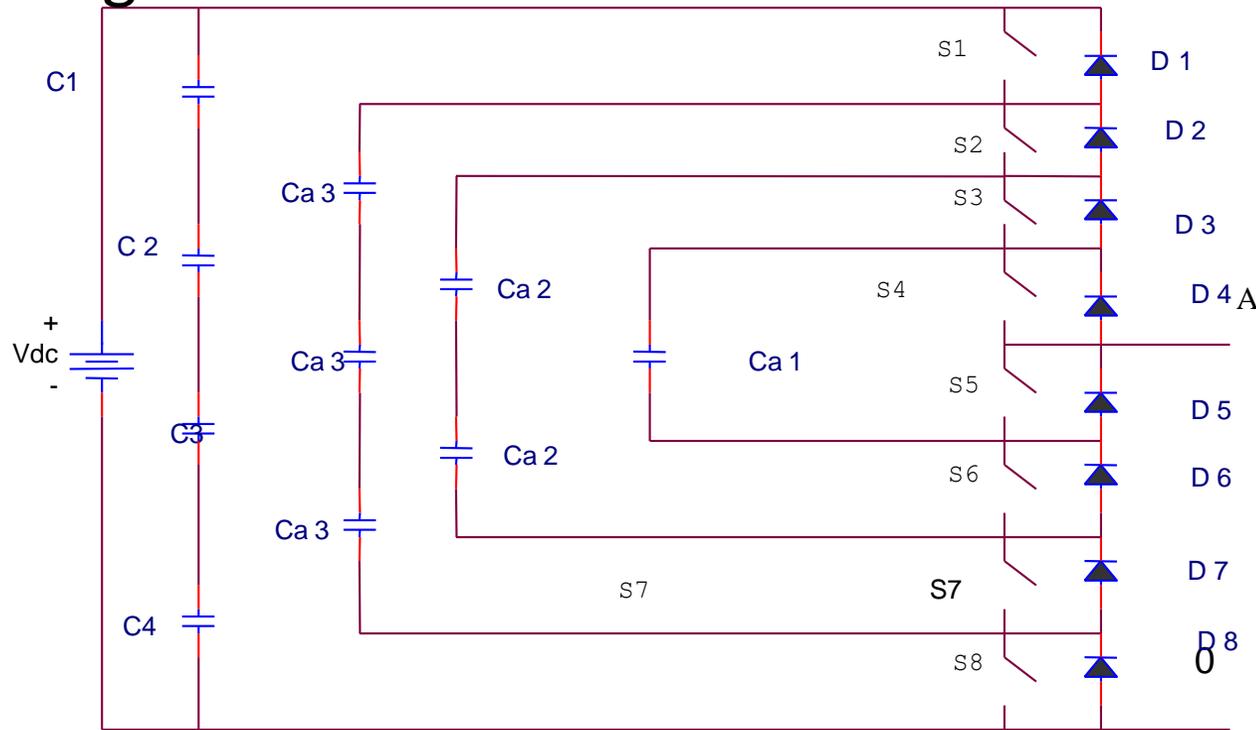
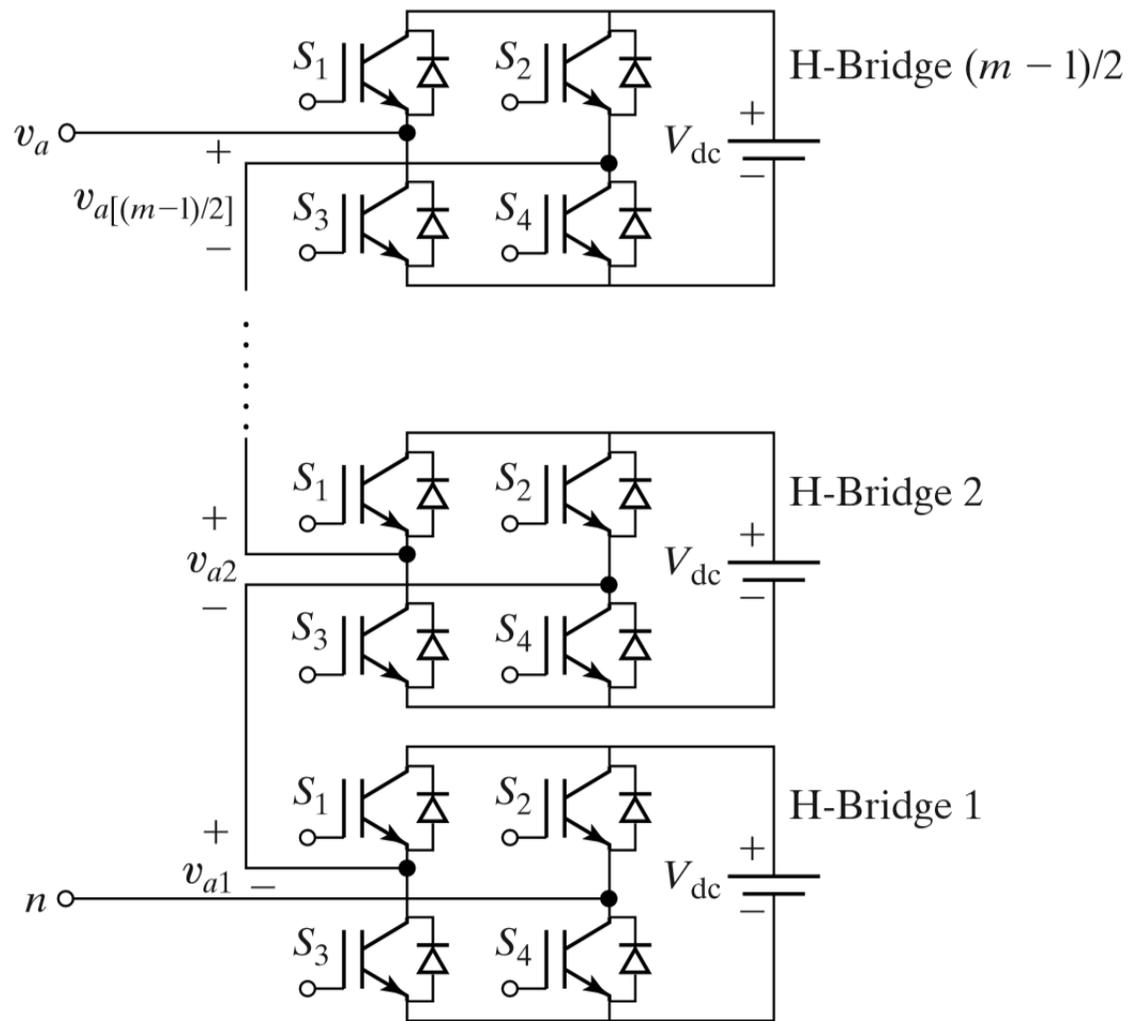


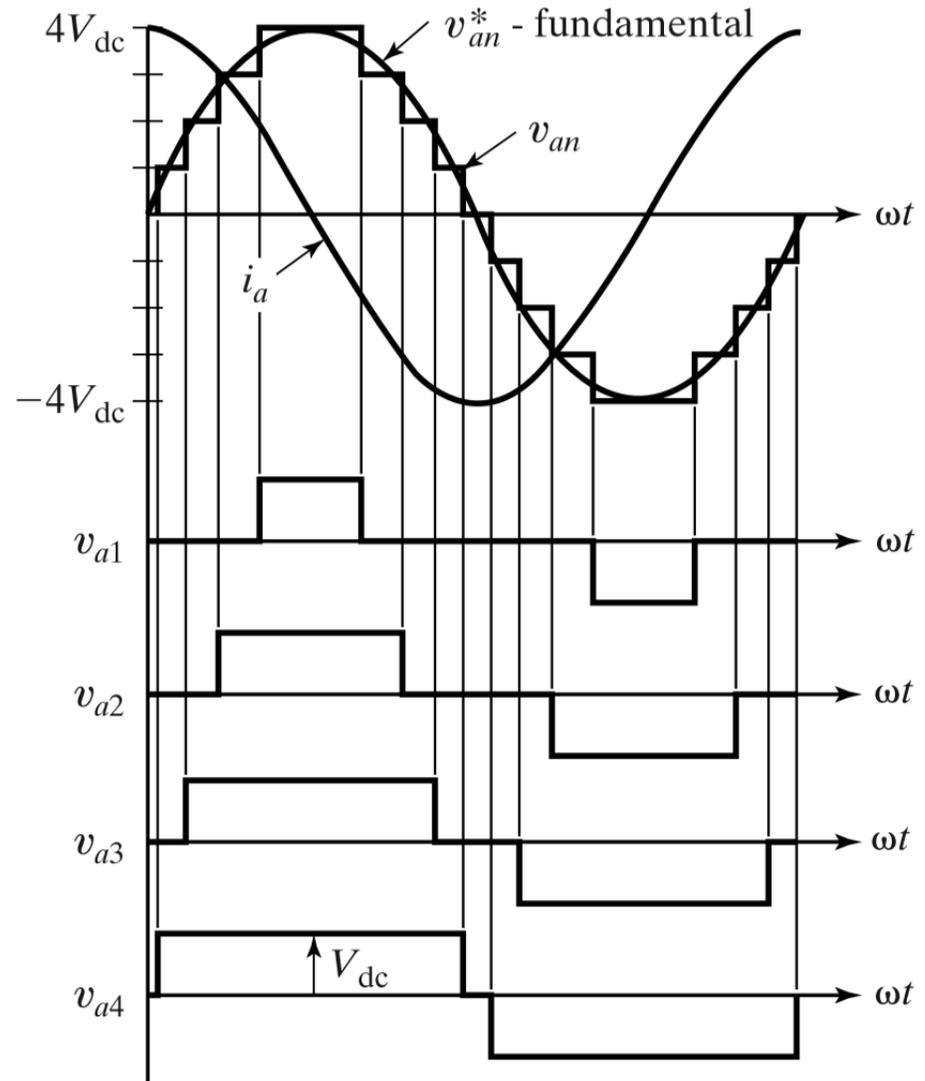
Fig. (6) A five level flying-capacitor inverter

3-Multilevel inverter using cascaded–inverter with separate DC source

This type of inverter consists of full bridge or H-Bridge inverters connected in series and the output voltage is equal to the sum of the output of each full–bridge, and each independent source may be obtained from either battery, or solar cell, or fuel cell, and the configuration is recently become popular in ac power supplies, and adjustable speed drive applications. And this type has less components than the other inverter types, and can avoid extra clamping diode for (DCMI), and voltage balancing capacitor for (FCMI). Fig. (7) shows a single phase configuration, in which each DC source is associated with single phase H-bridge inverter, the output of each H-bridge can be controlled by four switches. The



(a) Circuit diagram



(b) Output waveform of nine-level phase voltage

single phase cascade inverter configuration

Full bridge (single phase) is built from a two half-bridge legs , the switching in the second leg is “delayed by 180 degrees” from the first leg. H-bridges are connected in series so that to generate m-level a.c output waveform, and the synthesizes output waveform is the sum of each H-bridge level, and the number of levels can be defined as:

$$m= 2s+1 \tag{.1}$$

Where s is the number of dc source

For example a 11-level output can be obtained by connecting five H-bridge cells in series. In Fig. (8) shows a single – phase configuration for m-level cascaded multilevel inverter, and the output voltage is given as:

$$V_{an}=V_1+V_2+V_3+-----+V_{(m-1)}/2 \tag{.2}$$

Because the zero voltage is common for all inverter output, the total number of levels become $2s+1$

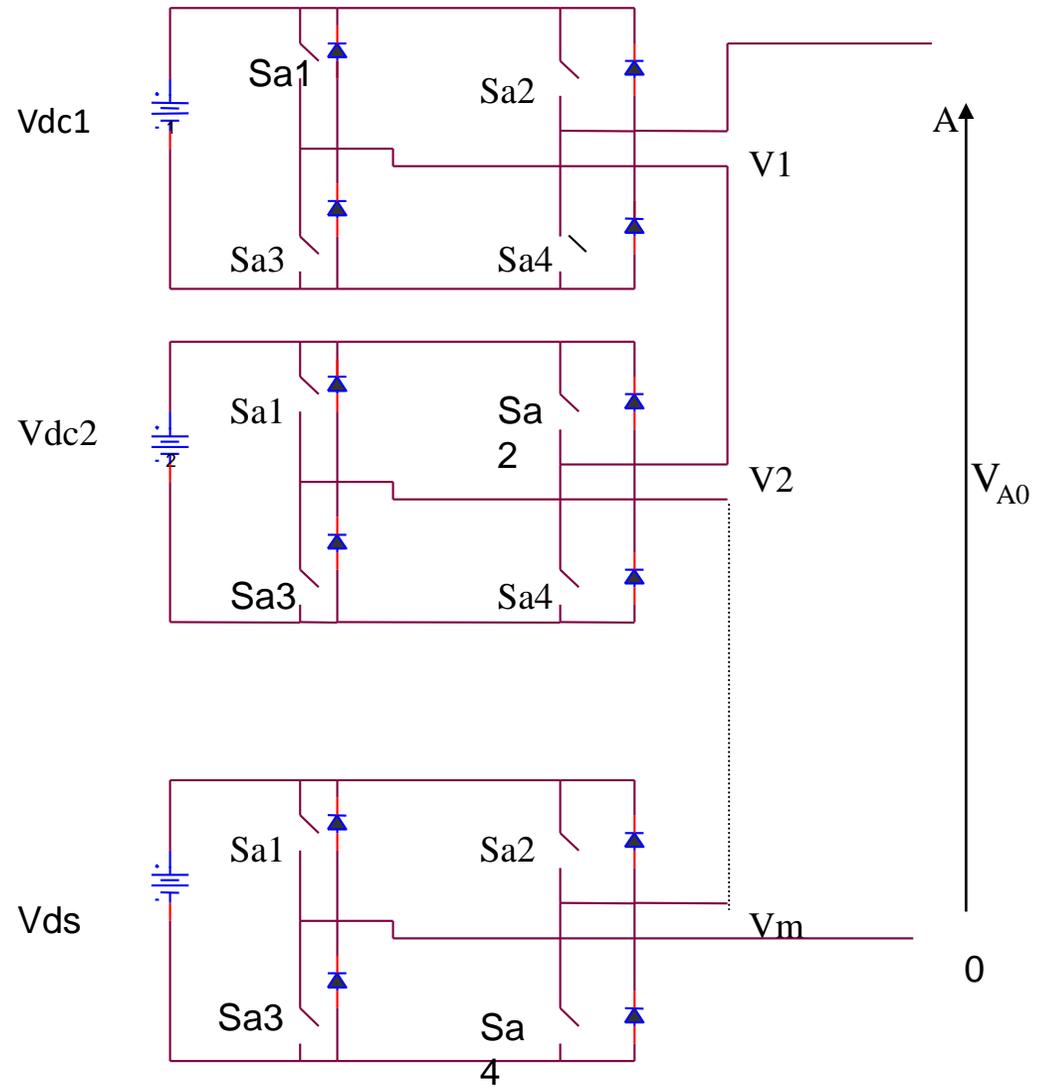


Fig. (8) single phase configuration for m-level cascaded inverter

An example of seven-level cascaded inverter and the corresponding H-bridge cell output waveform is shown in Fig. (9), for equal dc source.

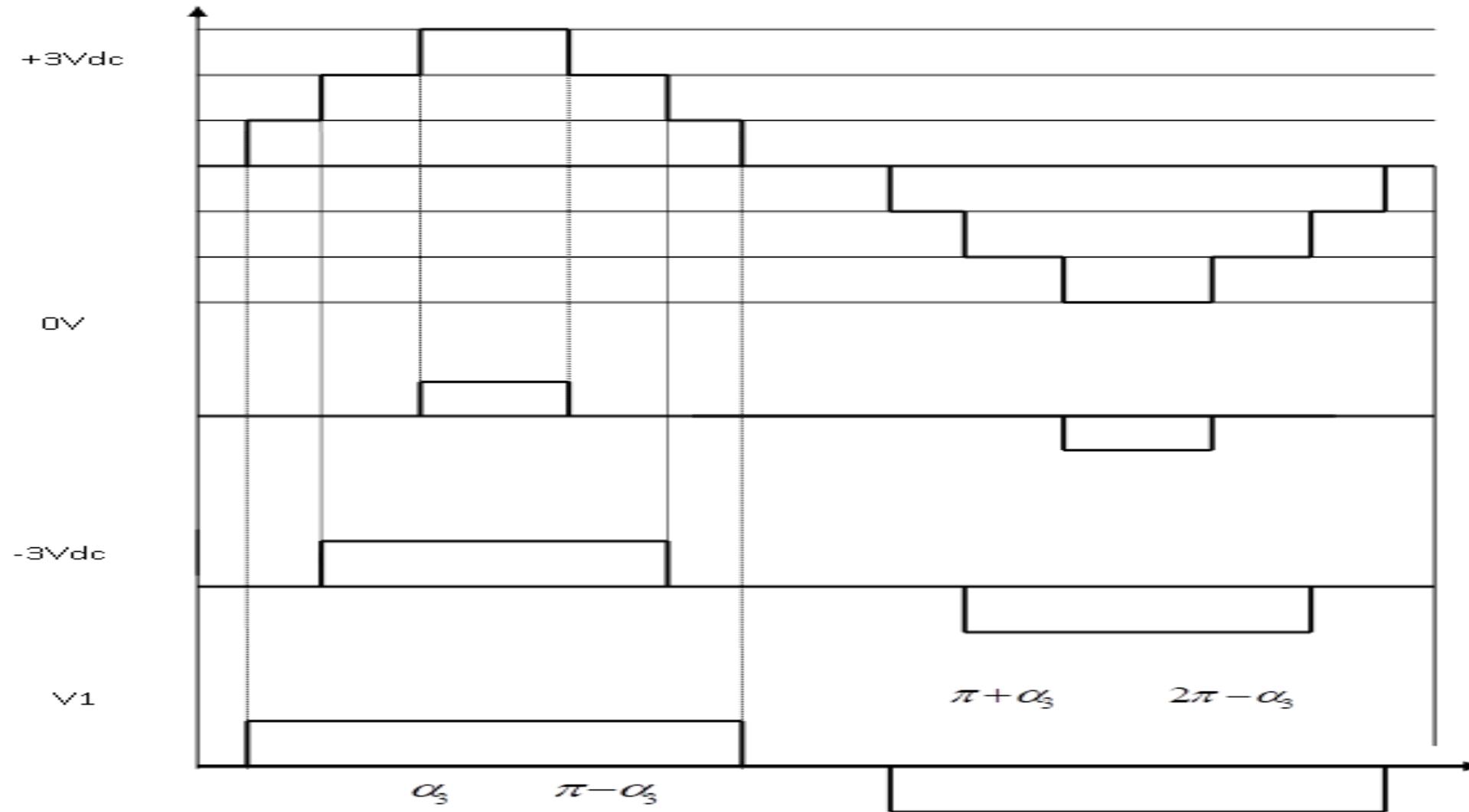


Fig. (9) waveform showing a 7-level output voltage and each H-bridge output voltage

OPTIMIZED HARMONIC STEEPED WAVEFORM TECHNIQUE (OHSW)

There is a considerable complicity in tread-off when choosing the number of voltage steps. Consider Fig. (10), based on the circuit complication and control possibilities, there are three possible optimization techniques exist to reduce the low order harmonics, in order to reduce the harmonic distortion as much as possible in the output waveform :

- 1) Assuming equally spaced steps, step heights are optimized.
- 2) Assuming the steps of equal heights, their spacing are optimized
- 3) Optimizing both heights and spacing .

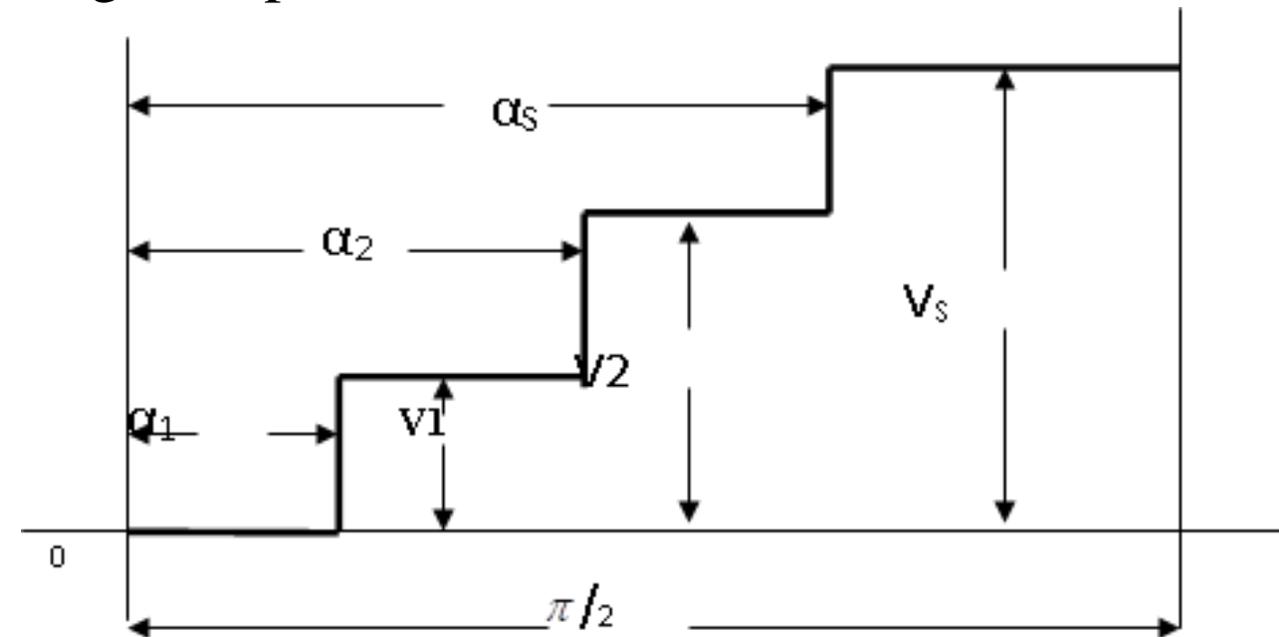


Fig. (10) Generalized steeped waveform

the method used to solve the appropriated switching angles of the Optimized Harmonic Stepped-Waveform (OHSW) technique will be presented for cascaded-inverter using separated dc sources (SDCSs) is considered.

As shown in Fig. (11), H-bridge cells are connected in series, and the output voltage waveform is the sum of the voltage waveform of each H-bridge.

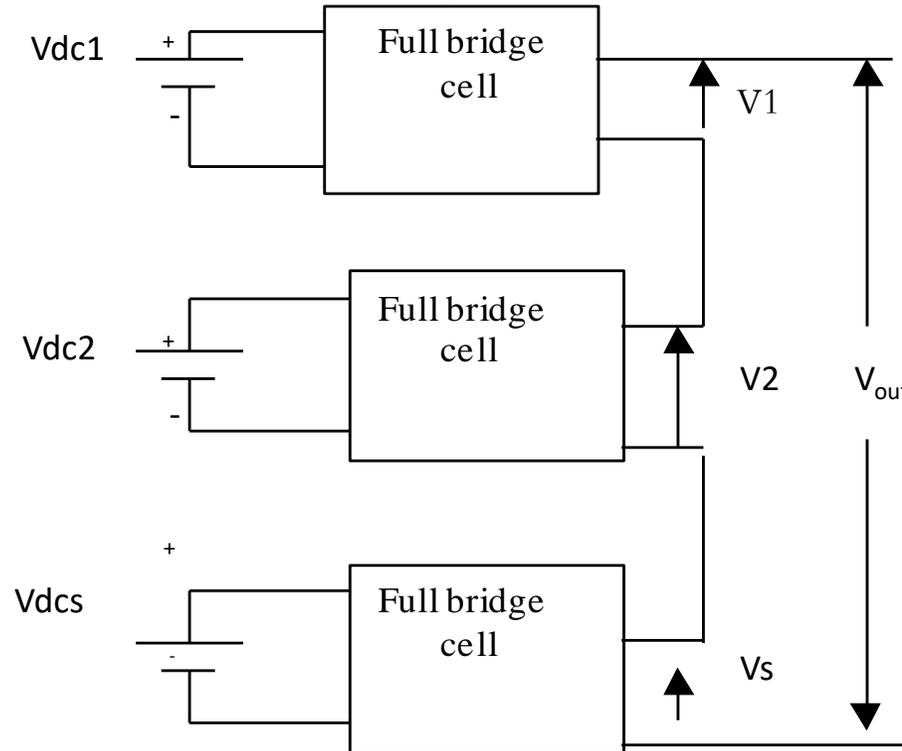


Fig. (11) Schematic diagram of an s H-bridges single phase cascaded multilevel inverter

$$V_{out} = V_1 + V_2 + \dots + V_s \quad (4)$$

A $2s+1$ levels can be synthesized with s H-bridge cells and s separate dc sources (SDCSs). Fig (12) illustrate a general waveform of s H-bridge cells multilevel inverter.

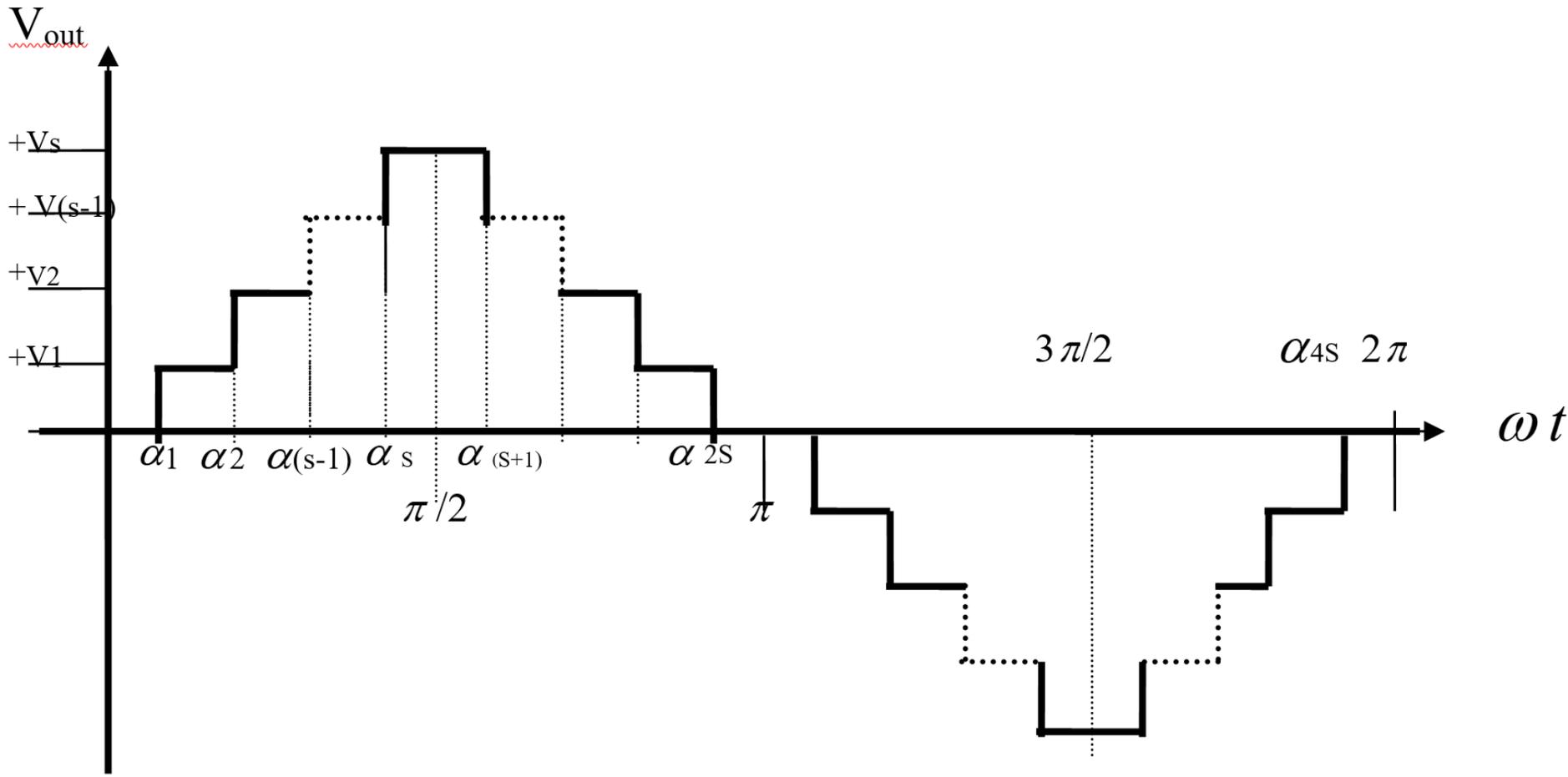


Fig. (12) output voltage waveform of s H-bridge cells multilevel inverter inverter.

In general the modulation index M of the SPWM is the ratio of the modulating signal amplitude to the carrier signal amplitude, while For the specified multilevel inverter case the modulation index is define as follow:

$$M = \frac{V_L^*}{V_{L \max}}$$

Where

V_L^* is the amplitude command of the inverter output voltage

$V_{L \max}$ is the maximum attainable amplitude of the converter i.e

$V_{L \max} = s \cdot V_{dc}$, s is the number of dc source, or H-bridge cells

the Fourier series of the quarter-wave symmetric s H-bridge cell multilevel waveform is written as follows: (HW)

$$b_n = \frac{4E}{n\pi} \sum_{K=1}^S \cos(n\alpha_k)$$

$$V_{out}(\omega t) = \sum_{n=1}^{\infty} \left[\frac{4E}{n\pi} \sum_{k=1}^S \cos(n\alpha_k) \right] \sin(n\omega t)$$

Where

α_K is the switching angle, which must satisfy the following condition

$$\alpha_1, \alpha_2, \alpha_3, \dots, \alpha_S < \frac{\pi}{2}$$

s is the number of H-bridge cells.

n is the odd harmonic order.

E is the amplitude of dc voltage.

Example. A single phase 7-level cascaded inverter has $f=50$ Hz, each separate dc source $V_{dc1} = V_{dc2} = V_{dc3} = 100V$. The switching angles designed so that the value $\alpha_1 = 13.22^\circ$, $\alpha_2 = 38^\circ$ and $\alpha_3 = 82.9^\circ$.

1- Express load current in Fourier series up to 11th harmonic assume $R=5\Omega$, $L=20mH$

2- Calculate the value of the total

$$b_n = \frac{4E}{n\pi} \sum_{k=1}^S \cos(n\alpha_k) \quad V_{out}(\omega t) = \sum_{n=1}^{\infty} \left[\frac{4E}{n\pi} \sum_{k=1}^S \cos(n\alpha_k) \right] \sin(n\omega t)$$

$$V_1 = \frac{4 \times 100}{1 \times \pi} [\cos(1 \times \alpha_1) + \cos(1 \times \alpha_2) + \cos(1 \times \alpha_3)] = 240.1V$$

$$V_3 = \frac{4 \times 100}{3 \times \pi} [\cos(3 \times \alpha_1) + \cos(3 \times \alpha_2) + \cos(3 \times \alpha_3)] = 0$$

$$V_5 = \frac{4 \times 100}{5 \times \pi} [\cos(5 \times \alpha_1) + \cos(5 \times \alpha_2) + \cos(5 \times \alpha_3)] = 0$$

$$V_7 = \frac{4 \times 100}{7 \times \pi} [\cos(7 \times \alpha_1) + \cos(7 \times \alpha_2) + \cos(7 \times \alpha_3)] = -15.94717V$$

$$V_9 = \frac{4 \times 100}{9 \times \pi} [\cos(9 \times \alpha_1) + \cos(9 \times \alpha_2) + \cos(9 \times \alpha_3)] = 19.2V$$

$$V_{11} = \frac{4 \times 100}{11 \times \pi} [\cos(11 \times \alpha_1) + \cos(11 \times \alpha_2) + \cos(11 \times \alpha_3)] = -14.7V$$

$$V_{out} = 240 \sin(1 \times 314t) - 15.9 \sin(7 \times 314t) + 19.2 \sin(9 \times 314t) + 14.7 \sin(11 \times 314t)$$

$$I_{out} = \frac{240}{z_1} \sin(1 \times 314t - \theta_1) - \frac{15.9}{z_7} \sin(7 \times 314t - \theta_7) + \frac{19.2}{z_9} \sin(9 \times 314t - \theta_9) - \frac{14.7}{z_{11}} \sin(11 \times 314t - \theta_{11})$$

Where

$$z_n = \sqrt{R^2 + (n\omega L)^2}$$

$$\theta_n = \tan^{-1} \frac{n\omega L}{R}$$

| n | Zn | θ_n |
|----|------|------------|
| 1 | 8 | 58 |
| 7 | 44 | 83.5 |
| 9 | 56.7 | 84.9 |
| 11 | 69.2 | 85.8 |

$$I_{out} = 30 \sin(314t - 58) - 0.361 \sin(7 \times 314t - 83.5) + 0.338 \sin(9 \times 314t - 84.9) - 0.212 \sin(11 \times 314t - 85.8)$$

$$THD = \frac{\sqrt{0.361^2 + 0.338^2 + 0.212^2}}{30} = \frac{0.538}{30} = 1.795\%$$

Ac motors exhibit highly coupled, nonlinear, and multivariable structures as opposed to much simpler decoupled structures of separately excited dc motors. The control of ac drives generally requires complex control algorithms that can be performed by microprocessors or microcomputers along with fast-switching power converters. The ac motors have a number of advantages; they are lightweight (20% to 40% lighter than equivalent dc motors), are inexpensive, and have low maintenance compared with dc motors. They require control of frequency, voltage, and current for variable-speed applications. The power converters, inverters, and ac voltage controllers can control the frequency, voltage, or current to meet the drive requirements. These power controllers, which are relatively complex and more expensive, require advanced feedback control techniques such as model reference, adaptive control, sliding mode control, and field-oriented control. However, the advantages of ac drives outweigh the disadvantages. There are four types of ac drives: 1. Induction motor drives. 2. Synchronous motor drives. 3. Stepper motor drives. 4. Linear induction motor. Ac drives are replacing dc drives and are used in many industrial and domestic