الكلية	الهندسة
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المادة باللغة الانجليزية	Electronic Devices and Circuit Theory
المادة باللغة العربية	مكونات و دوائر إلكترونية
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عنوان المحاضرة باللغة الانجليزية	**Diode Applications**
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Lecture 4

Diode Applications

4.1 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The diode analysis will now be expanded to include time-varying functions such as the sinusoidal waveform and the square wave. The simplest of networks to examine with a time-varying signal appears in Figure 1

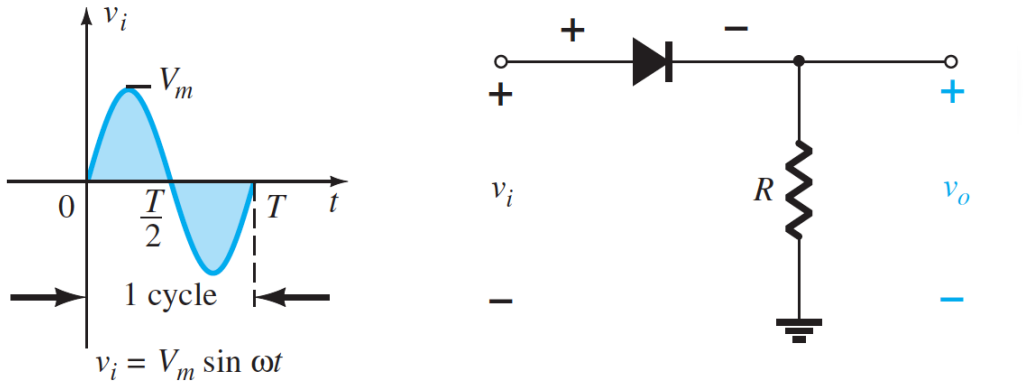


Figure 1: Half-Wave Rectifier

Over one full cycle, defined by the period T of Figure 1 , the average value (the algebraic sum of the areas above and below the axis) is zero. The circuit of Figure 1, called a half-wave rectifier, will generate a waveform v_o that will have an average value of particular use in the ac-to-dc conversion process.

During the interval $t = 0 \rightarrow T/2$ in Figure 1 the polarity of the applied voltage v_i is such as to establish "pressure" in the direction indicated and turn on the diode with the polarity appearing above the diode (See Figure 2).

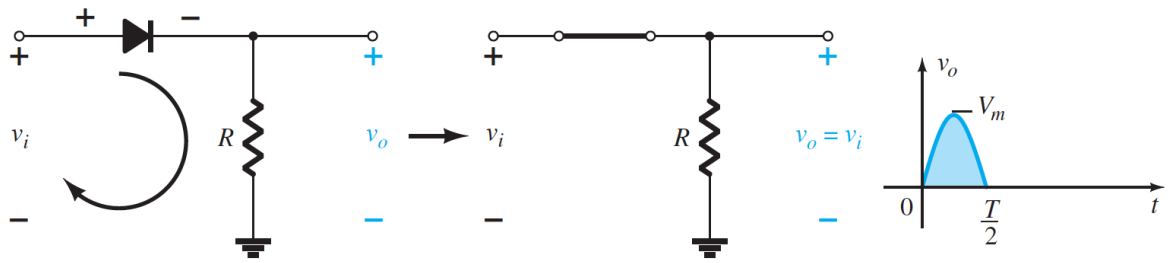


Figure 2: Conduction region ($0 \rightarrow T/2$).

For second half $t = T/2 \rightarrow T$, see Figure 3

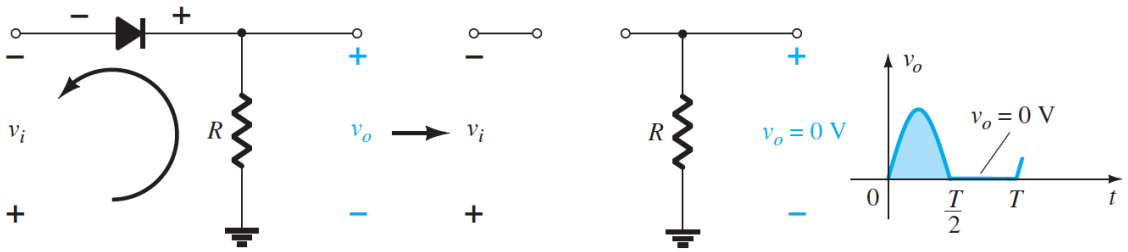


Figure 3: Conduction region ($T/2 \rightarrow T$).

The output signal v_o now has a net positive area above the axis over a full period and an average value determined by

$$V_{dc} = 0.318\, V_m$$ half-wave

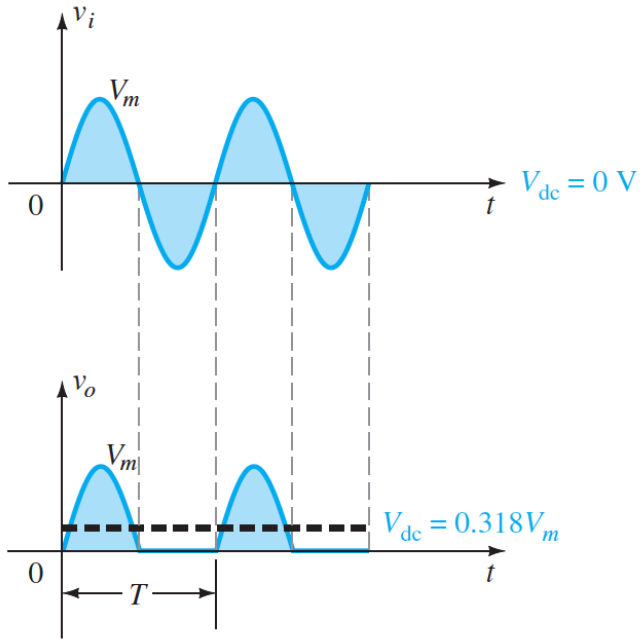


Figure 4: Half-wave rectified signal.

The process of removing one-half the input signal to establish a dc level is called *halfwave rectification*.

The effect of using a silicon diode with $V_K = 0.7$ V is demonstrated in Figure 5 for the forward-bias region.

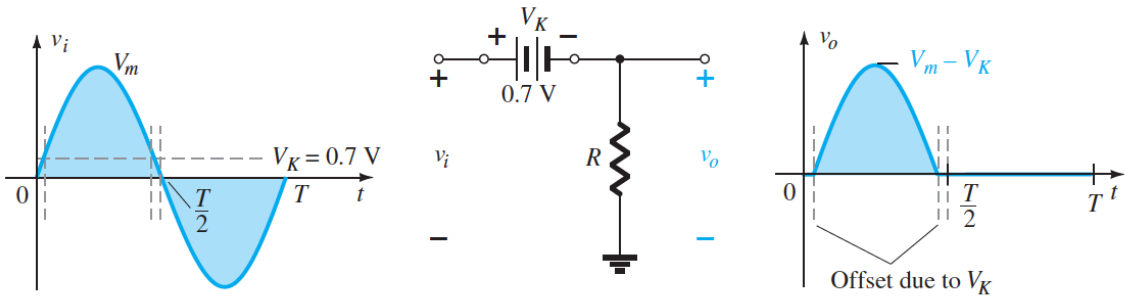


Figure 5: Effect of V_K on half-wave rectified signal.

And the value of V_{dc} is

$$V_{dc} \cong 0.318(V_m - V_K)$$

EXAMPLE 2.16

a. Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.49.
b. Repeat part (a) if the ideal diode is replaced by a silicon diode.
c. Repeat parts (a) and (b) if V_m is increased to 200 V, and compare solutions using Eqs. (2.7) and (2.8).

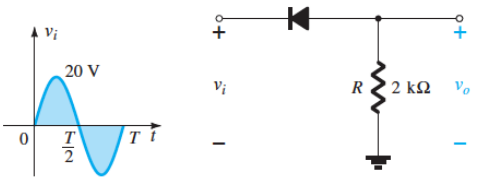


FIG. 2.49
Network for Example 2.16.

Solution:

a. In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.50, and v_o will appear as shown in the same figure. For the full period, the dc level is

$$V_{dc} = -0.318V_m = -0.318(20\text{ V}) = \mathbf{-6.36\text{ V}}$$

The negative sign indicates that the polarity of the output is opposite to the defined polarity of Fig. 2.49.

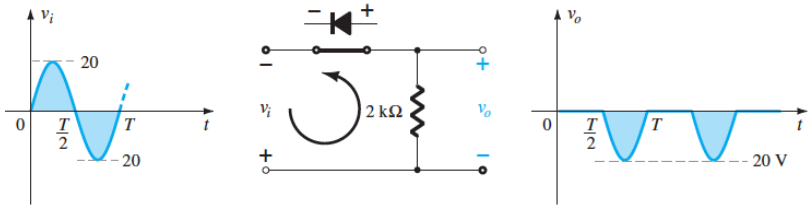


FIG. 2.50
Resulting v_o for the circuit of Example 2.16.

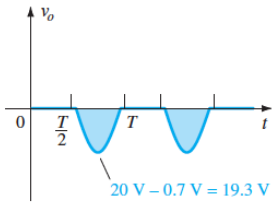


FIG. 2.51
Effect of V_K on output of Fig. 2.50.

b. For a silicon diode, the output has the appearance of Fig. 2.51, and

$$V_{dc} \cong -0.318(V_m - 0.7\text{ V}) = -0.318(19.3\text{ V}) \cong \mathbf{-6.14\text{ V}}$$

The resulting drop in dc level is 0.22 V, or about 3.5%.

c. Eq. (2.7): $V_{dc} = -0.318\,V_m = -0.318(200\text{ V}) = \mathbf{-63.6\text{ V}}$

Eq. (2.8): $V_{dc} = -0.318(V_m - V_K) = -0.318(200\text{ V} - 0.7\text{ V})$

$= -(0.318)(199.3\text{ V}) = \mathbf{-63.38\text{ V}}$

which is a difference that can certainly be ignored for most applications. For part (c) the offset and drop in amplitude due to V_K would not be discernible on a typical oscilloscope if the full pattern is displayed.

4.2 PIV (PRV)

The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse bias region or the diode will enter the *Zener avalanche region*.

PIV rating $\geqq V_m$ half-wave rectifier

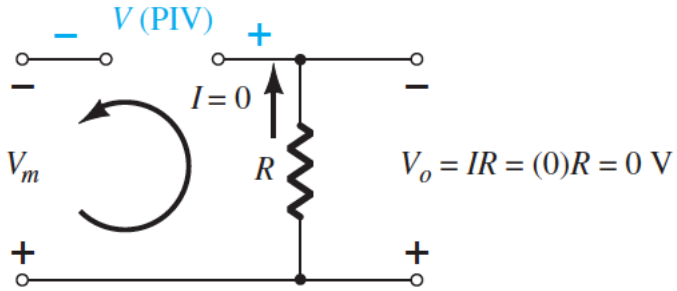


Figure 6:Determining the required PIV rating for the

4.3 SINUSOIDAL INPUTS; FULL-WAVE RECTIFICATION

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification*. The most familiar network for performing such a function appears in Figure 7 with its four diodes in a bridge configuration

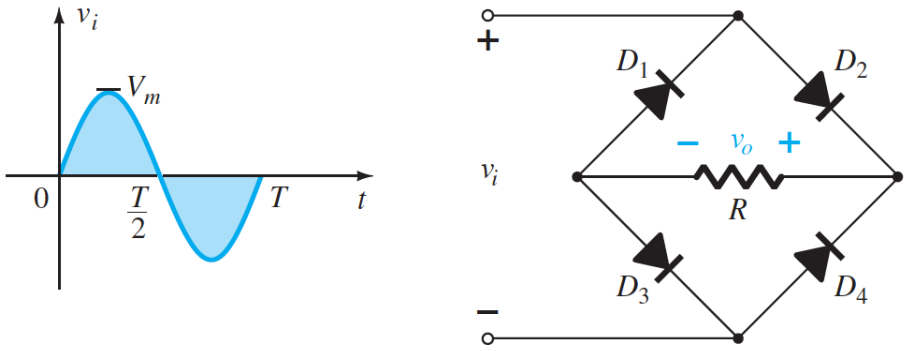


Figure 7: Full-wave bridge rectifier.

During the period t=0 to T >2 the polarity of the input is as shown in Figure 8

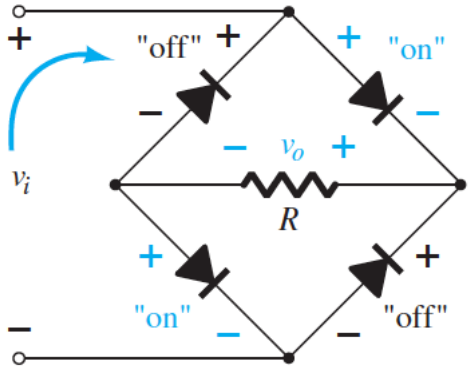


Figure 8: Network of Figure 7 for the period 0 to T/2 of the input voltage v_i

The net result is the configuration of Figure 9 , with its indicated current and polarity across R. Since the diodes are ideal, the load voltage is $v_o = v_i$, as shown in the same figure.

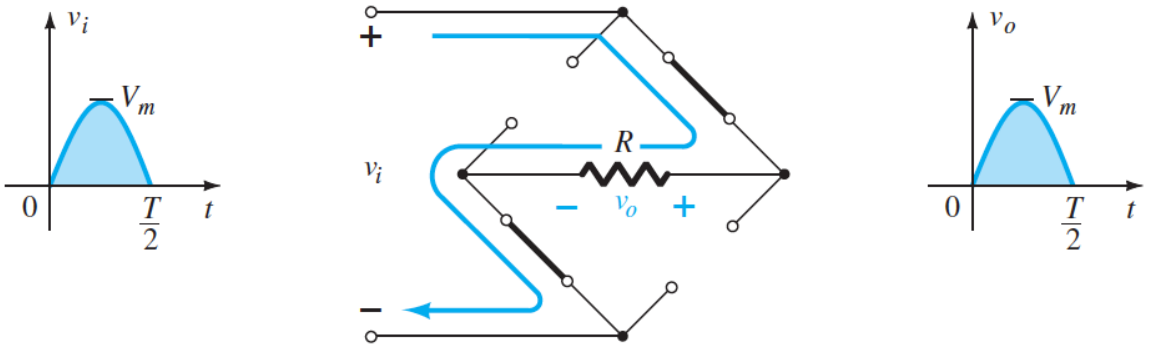


Figure 9: Conduction path for the positive region of v_i .

For the negative region of the input the conducting diodes are D1 and D4, resulting in the configuration of Figure 10.

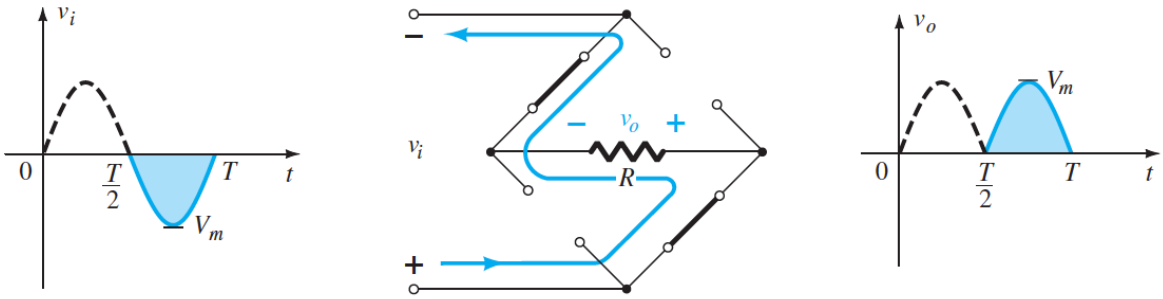


Figure 10:Conduction path for the negative region of v_i .

Over one full cycle the input and output voltages will appear as shown in Figure 11.

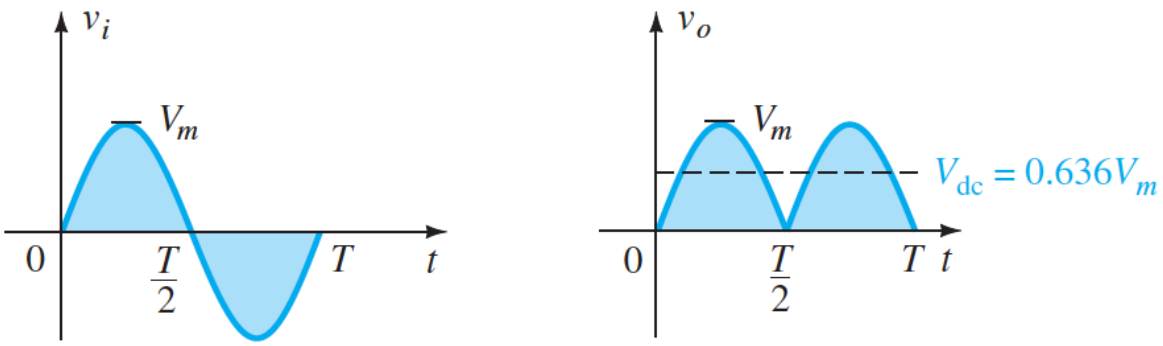


Figure 11: Input and output waveforms for a full-wave rectifier.

$$V_{dc} = 2(0.318\,V_m)$$

$$\boxed{V_{dc} = 0.636\,V_m}$$ full-wave

If silicon rather than ideal diodes are employed as shown in Figure 12, the application of Kirchhoff's voltage law around the conduction path results in

$$v_i - V_K - v_o - V_K = 0$$

$$v_o = v_i - 2V_K$$

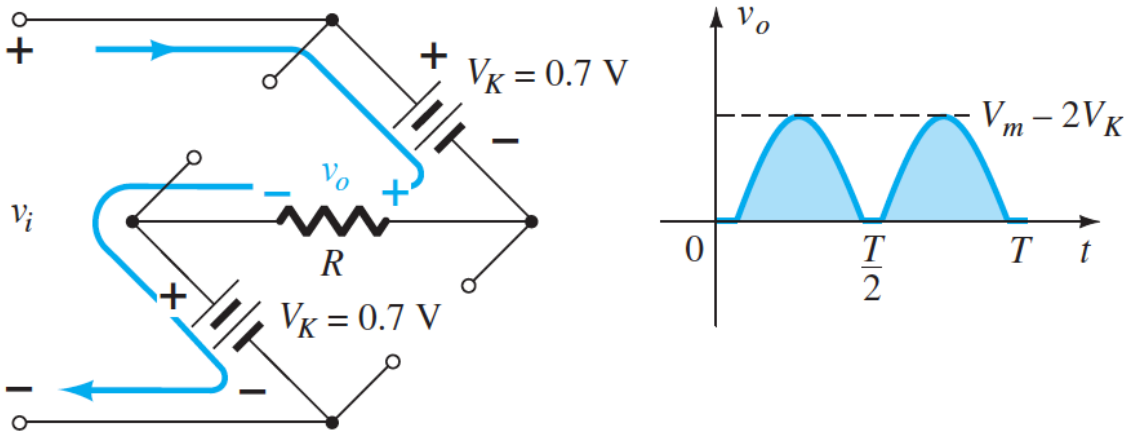


Figure 12: Determining V_{omax} for silicon diodes in the bridge configuration.

The peak value of the output voltage v_o is therefore

$$V_{o_{\max}} = V_m - 2V_K$$

The following equation can be applied for the average value with a relatively high level of accuracy

$$V_{\text{dc}} \cong 0.636(V_m - 2V_K)$$

PIV The required PIV of each diode (ideal) can be determined from Figure 13 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across R is V m and the PIV rating is defined by

$$\text{PIV} \geqq V_m$$ full-wave bridge rectifier

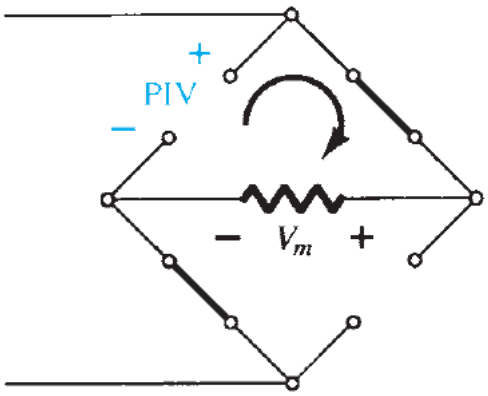


Figure 13:Determining the required PIV for the bridge configuration.

Center-Tapped Transformer

A second popular full-wave rectifier appears in Figure 14 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer.

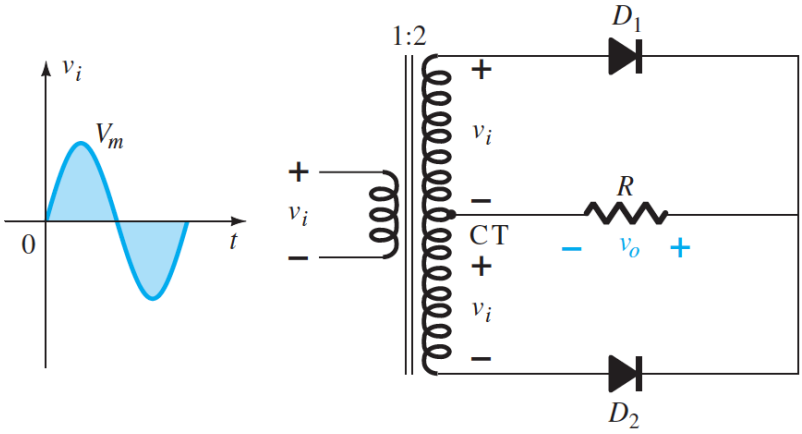


Figure 14: Center-tapped transformer full-wave rectifier.

During the positive portion of v_i applied to the primary of the transformer, the network will appear as shown in Figure 15 with a positive pulse across each section of the secondary coil.

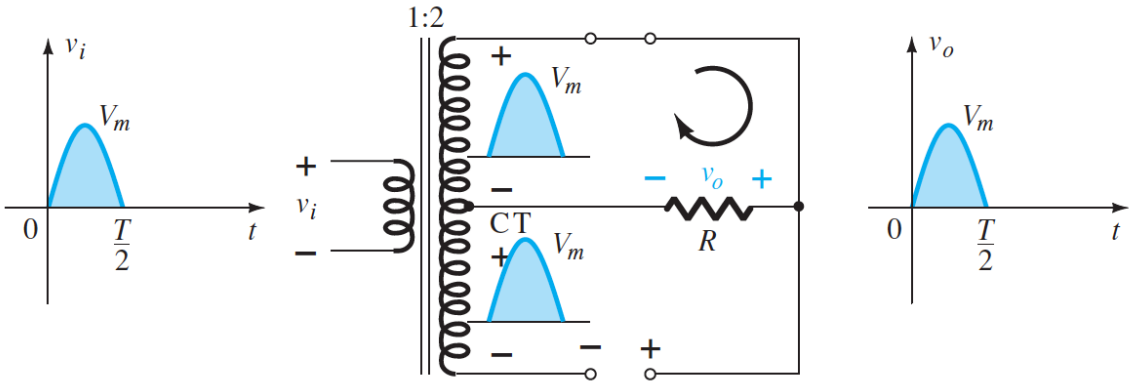


Figure 15:Network conditions for the positive region of v_i .

During the negative portion of the input the network appears as shown in Figure 16, reversing the roles of the diodes but maintaining the same polarity for the voltage across the load resistor R.

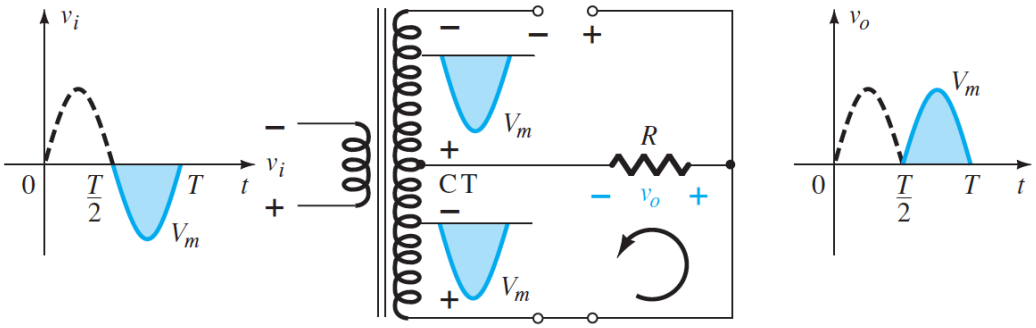
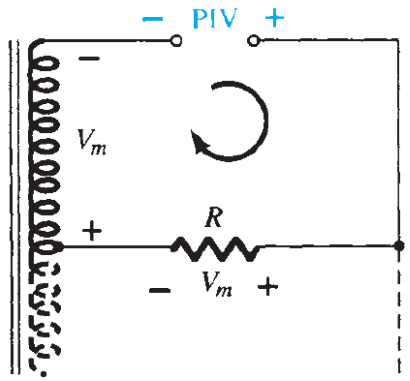


Figure 16:Network conditions for the negative region of v_i .

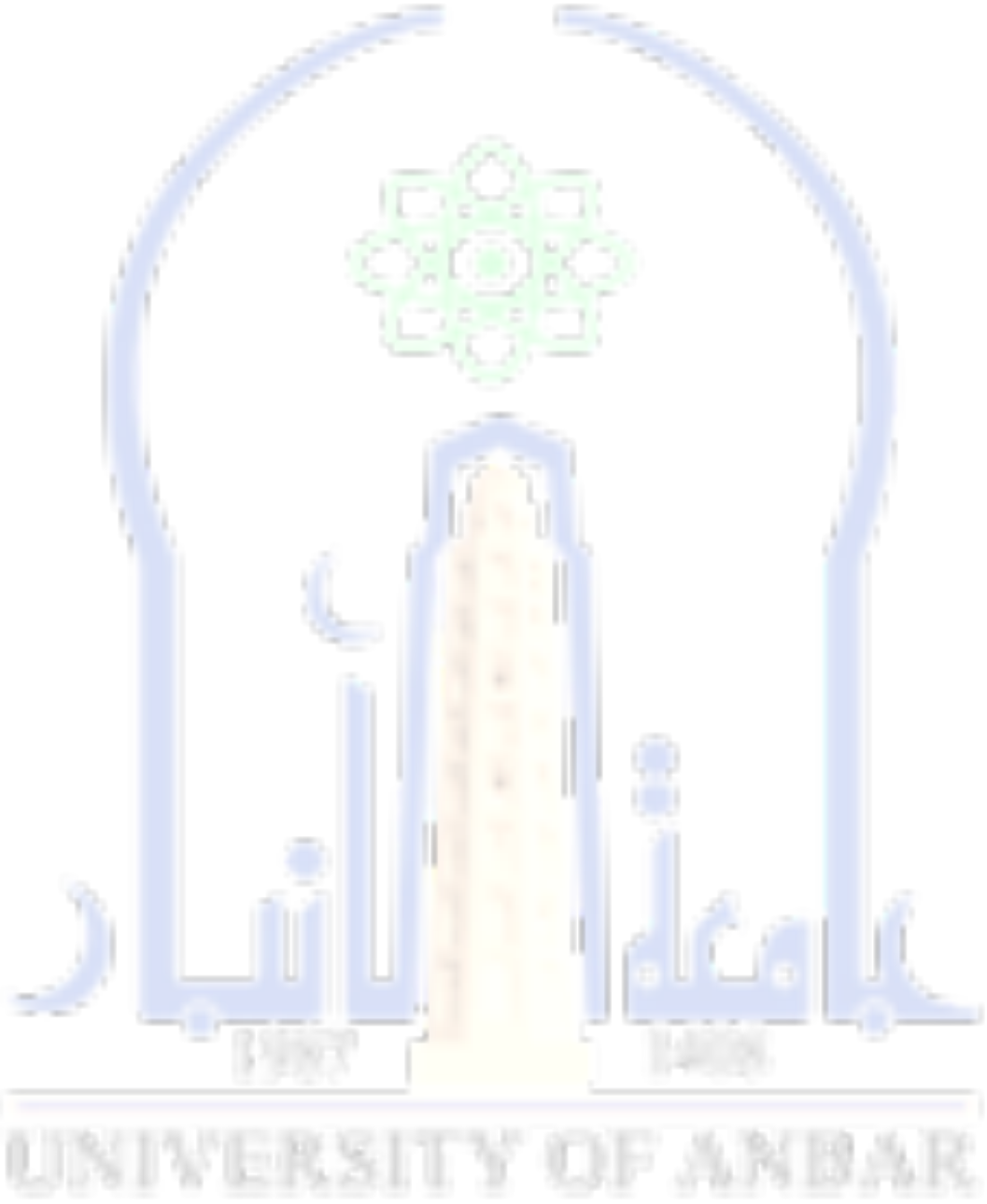
PIV The network of Figure 17 will help us determine the net PIV for each diode for this full-wave rectifier.



$$\text{PIV} = V_{\text{secondary}} + V_R$$
$$= V_m + V_m$$

$$\boxed{\text{PIV} \geqq 2V_m}$$ CT transformer, full-wave rectifier

Figure 17: Determining the PIV level for the diodes of the CT transformer full-wave rectifier.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