Chapter 19

PSK/QPSK SYSTEM

19.1 OBJECTIVES

1. To study the principle of PSK/QPSK modulation.
2. To study the principle of PSK/QPSK demodulation.
3. To implement PSK/QPSK modulator.
4. To implement PSK/QPSK demodulator.

19.2 DISCUSSION OF FUNDAMENTALS

PSK/QPSK Modulator

As mentioned in Chapter 18, phase-shift keying (PSK) modulation process may be viewed as the special case of phase modulation (PM). The PSK modulation is shown in Figure 19-1.

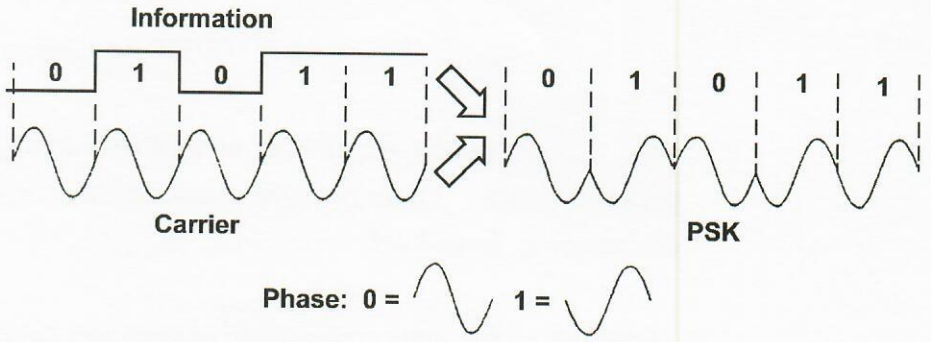

Figure 19-1 PSK modulation

In Figure 19-1, the carrier signal is a sinusoidal wave with fixed frequency and amplitude, the modulating signal is binary information. If input information is a low (0), the carrier signal maintains its phase. If input information is a high (1), the carrier reverses its phase by 180 degrees. The pair of sinusoidal waves that differ only in a relative phase-shift of 180 degrees are referred to as antipodal signals. This type of phase-shift keying is called binary PSK (BPSK) or phase-reverse keying (PRK).

As with BPSK, this modulation scheme is characterized by the fact that the information carried by the transmitted wave is contained in the phase. In particular, in quadriphase-shift keying (QPSK), the phase of the carrier takes on one of four equally spaced values, such as 0°, 90°, 180°, and 270°. Each possible value of the phase corresponds to a unique pair of bits called a dibit. For example, we may choose the forgoing set of phase values to represent the Gray-coded set of dibits: 00, 01, 11, and 10. The typical waveforms of QPSK modulation are shown in Figure 19-2.

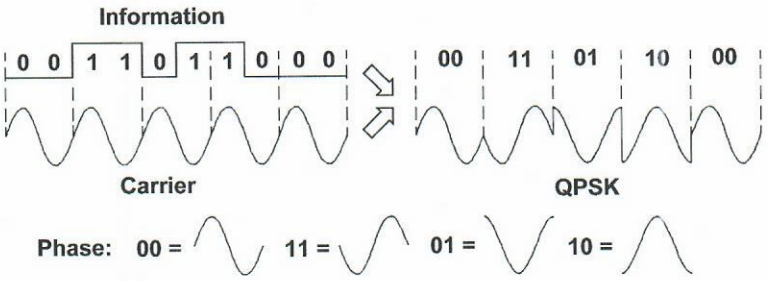

Figure 19-2 QPSK modulation

Note that the phase set of PSK and QPSK mentioned above is only a possible choice. Other possible phase-shifts of PSK and QPSK signals are shown in Table 19-1.

Table 19-1 Possible phase-shifts of PSK and QPSK

System	Information	Phase (degrees)		
		Learned	#1	#2
PSK	0	0	180	45
	1	180	0	225
QPSK	00	0	180	45
	11	180	0	225
	01	90	270	135
	10	270	90	315

Figure 19-3 shows a PSK/QPSK communication system. The modulator modulates the carrier signal by input information and produces a PSK or QPSK modulated signal. The modulated signal is transmitted through transmission medium, such as air, cable, and optical fiber, to the

input of demodulator. The demodulator receives PSK or QPSK transmitted signal and then reconstructs the original information data.

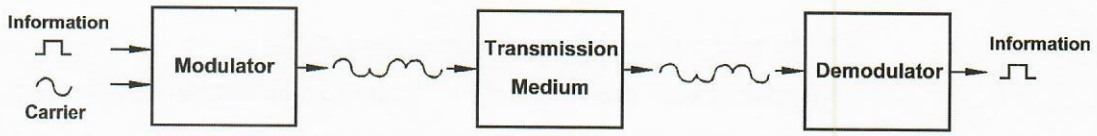

Figure 19-3 Block diagram of PSK/QPSK system

Figure 19-4 shows the functional blocks of a PSK/QPSK modulator. The carrier signal generator provides a carrier signal (sinusoidal wave) to the phase switching network and a square wave to the timing circuit. Phase-switching network provides four outputs (0°, 90°, 180°, 270°) to the inputs of data selector. The output X of data selector is determined by the select inputs A and B. There are four following cases:

1. If BA=00 (Q1=Q0=low), X=X0, the signal with phase shift 0°.
2. If BA=11 (Q1=Q0=high), X=X3, the signal with phase shift 180°.
3. If BA=01 (Q1=low, Q0=high), X=X1, the signal with phase shift 90°.
4. If BA=10 (Q1=high, Q0=low), X=X2, the signal with phase shift 270°.

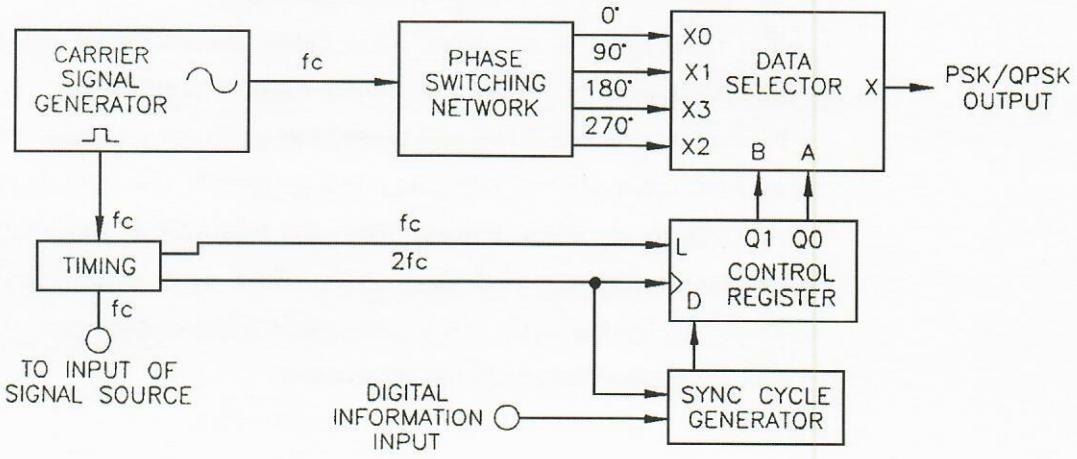

Figure 19-4 Block diagram of PSK/QPSK modulator

The timing circuit receives the square wave (fc) from the carrier signal generator output and produces two outputs: fc to the load control input and signal 2fc (twice the carrier frequency) to the clock input of control register as well as the sync cycle generator. These two signals of fc and 2fc and the data rate (measured in bits per second, bps) of input digital

information are used to determine whether the modulator operates in binary PSK or QPSK mode. There are three possible cases:

1. Bit rate = fc and no sync cycle generated

   In this case, the data rate is equal to the carrier frequency fc and the clock frequency is twice the carrier frequency 2fc. One bit of digital data stream is loaded into the control register two times. The outputs Q0-Q1 of control register are therefore the same, 00 or 11. The output X of data selector is either X0 or X3 input signal. This system operates in PSK mode.

2. Bit rate=2fc and no sync cycle generated

   In this case, data rate and clock frequency are equal to twice the carrier frequency, 2fc. Two bits of data stream are loaded to the control register each carrier cycle. The control register outputs Q0-Q1 may be 00, 01, 11, or 10. This system therefore operates in QPSK mode.

3. Bit rate = fc or 2fc, and sync cycle generated

   If a sync cycle is required, sync cycle control circuit will produce a control signal to control the output data of control shift register, and then a sync cycle signal will present at modulator output. The format of sync cycle shown in Figure 19-5 is used in our experiments. This sync cycle signal is different from the PSK/QPSK modulated signals shown in Figures 19-1 and 19-2. The sync cycle signal can be identified by the sync cycle detector in PSK/QPSK demodulator and can be viewed as an identification word.

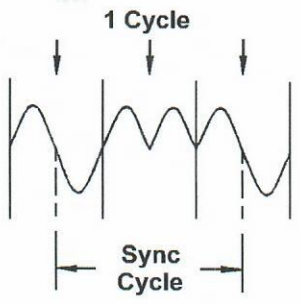

Figure 19-5 Synchronization cycle

PSK/QPSK Demodulator

There are many methods and circuits used to reconstruct the information (modulating signal) from PSK/QPSK modulated signal. In typical PSK/QPSK demodulator, PLL circuit is required for reconstructing clock signal that is used in modulator.

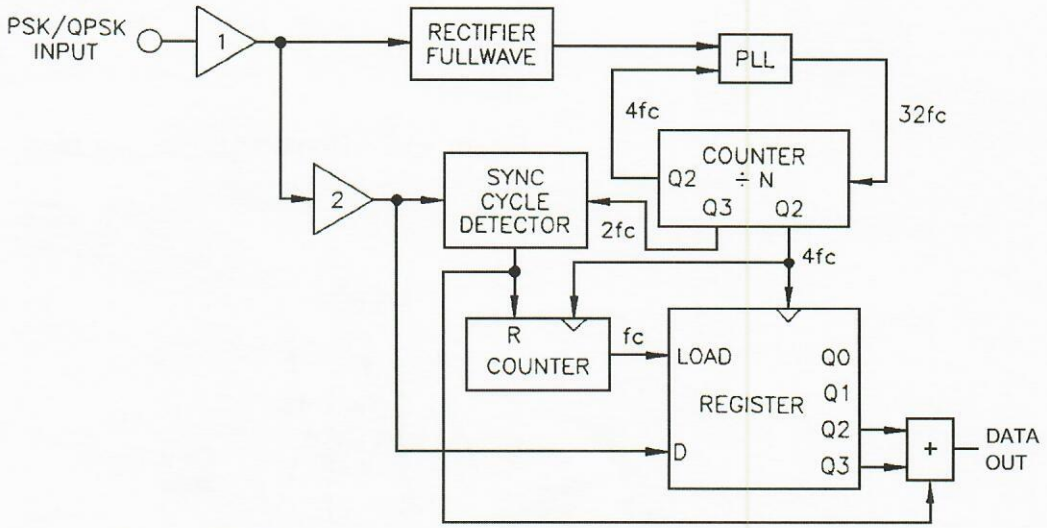

Figure 19-6 Block diagram of PSK/QPSK demodulator

Figure 19-6 shows the block diagram of PSK/QPSK demodulator. PSK/QPSK input signal is amplified by amplifier 1 and then rectified by full-wave rectifier, then the rectified pulse is connected to the input of the phase detector in PLL. This signal is used to reconstruct the clock signal.

Figure 19-7 shows the demodulator output data that is recovered from the received PSK/QPSK signal. From Figure 19-6, we see that various clock frequencies are produced by the PLL and divide-by-N counter. These clock signals are used to reconstruct the information data and to convert sync cycle signal to sync cycle data.

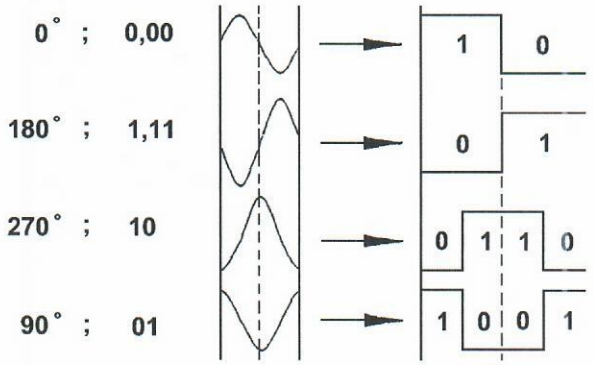

Figure 19-7 Demodulator output data

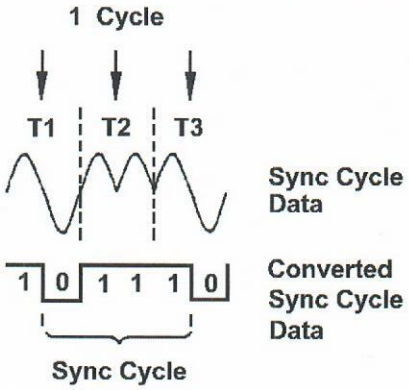

Figure 19-8 Sync cycle conversion

The sync cycle conversion is shown in Figure 19-8. The converted sync cycle data word is 0111. When the sync cycle detector receives this data word, a low is presented to indicate that a sync cycle is detected.

Practical Circuit Description

1. PSK/QPSK modulator

Figure 19-9 shows the schematic diagram of PSK/QPSK modulator. The precision waveform generator chip ICL8038 serves as the carrier signal generator that produces sinusoidal and square waves. The

frequency of the carrier generator is determined by the external timing resistors R2-R3 and capacitor C2 and is 7.1KHz approximately. Pins 7 and 8 are connected together to characterize the generator operating in VCO mode. The generated sinusoidal signal is connected to the inputs of phase switching network consisting of two noninverting amplifiers (U2a and U2d) and two inverting amplifiers (U2b and U2c). This phase-shift network provides four phase shifts 0°, 90°, 270°, and 180° to data inputs X0, X1, X2, and X3 of the data selector (U3), respectively. The output of data selector is determined by the state of select inputs A and B. Once the output is selected, the PSK/QPSK modulated signal is amplified by the non-inverting amplifier U8. The potentiometer VR5 is used to control the output amplitude of PSK/QPSK modulated signal.

The square wave present at U1 pin9 is connected to the input of timing circuit to generate a signal with the frequency 2fc twice the carrier frequency by the frequency doubling network constructed by U4b, U4c, and U5a and associated components R21, R22, C6, C7. The 2fc signal is connected to the clock inputs of the shift register U7 and the 4-bit binary counter U6a. The signal of the counter output Q0 is connected to inverters U4f and U4d and U7 pin1 (Load input). The frequency of this signal is fc. The modulating signal (digital information) is connected to DATA input (pin 2) of the control shift register U7. The outputs Q0-Q1 of the shift register are XORed with the signal on TP6, and then connected to the select inputs A and B of data selector.

Binary counters U6a and U6b are used to determine when to generate a sync cycle. The clock frequency of the binary counter U6a is 2fc. The output Q1 of U6a is connected to clock input of U6b, so that the clock frequency is fc/2 and the frequency of U6b Q3 is fc/32. The sync cycle is generated only in one-half duration of Q3 output signal or fc/16.

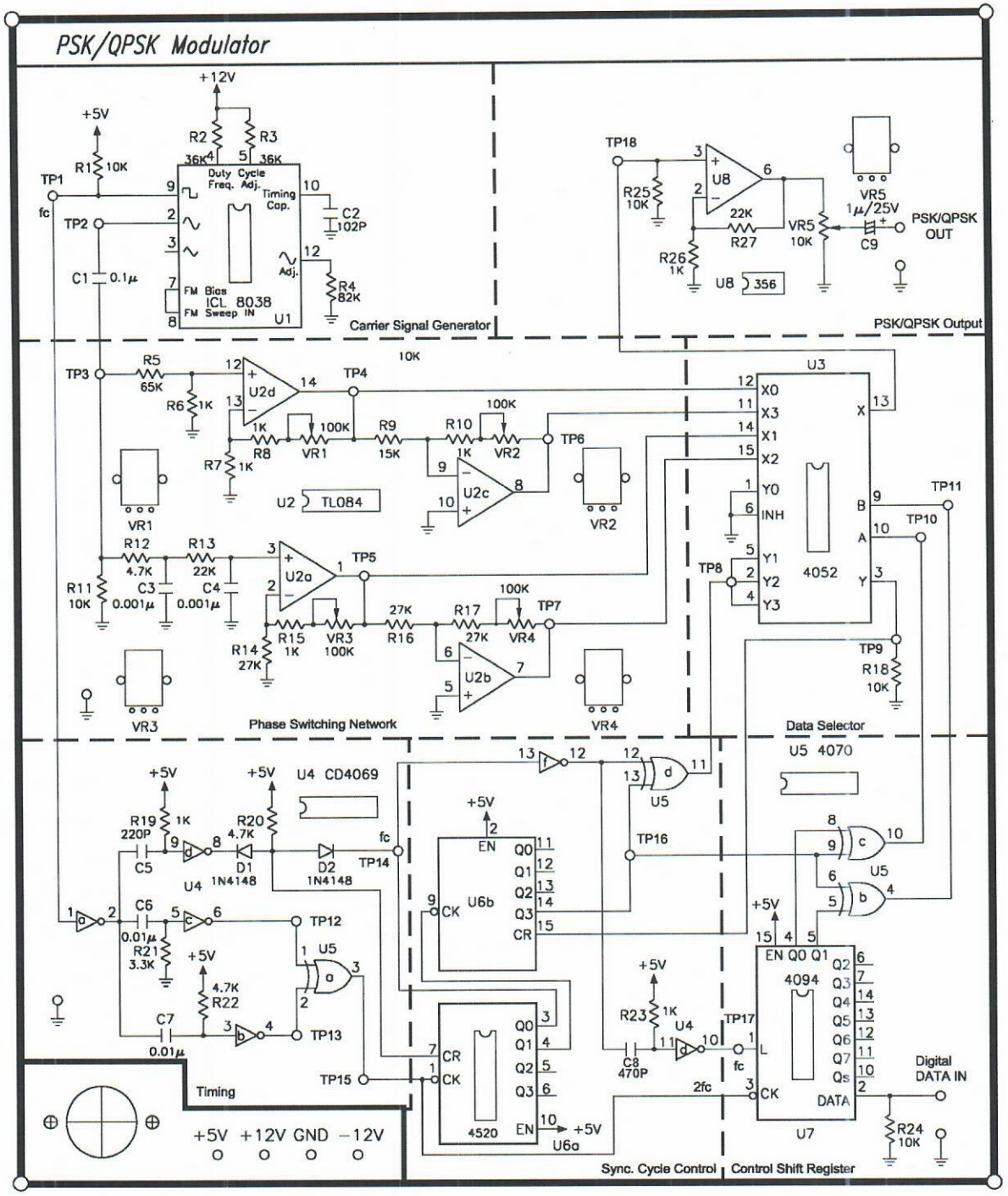

Figure 19-9 KL-94006 module

2. PSK/QPSK demodulator

Figure 19-10 shows the schematic diagram of PSK/QPSK demodulator. The amplifier U1d receives and amplifies the PSK/QPSK modulated signal for compensating the losses and improving the distortion caused by the transmission line. The full-wave rectifier, constructed by op amps U1c-U1b and diodes D1-D4, shapes the received PSK/QPSK signal to a positive-cycle signal, which is connected to the input of the phase detector in PLL (U2). VCO out signal (32fc) is the clock pulse of the divide-by-N counter. The counter produces two frequencies 4fc and 2fc on the outputs Q2 and Q3, respectively.

The amplified PSK/QPSK signal on U1d output terminal is connected to the input of amplifier U1a. U1a converts the PSK/QPSK signal to digital pulse signal as shown in Figure 19-7. This digital signal on TP5 is buffered by inverters U3e and U3f and then connected to the inputs J and K* of U4.

Sync cycle detector contains 4-stage register (U4) and 4-input NAND gate (U5b). The clock frequency of the register is 2fc. The reset pulse generated by the network (R21, C9, U3d) is used to clear the register outputs Q0-Q3. The digital data on TP5 is connected to the inputs J and K*. When a sync cycle is received, the register outputs Q3-Q0=0111, the output (TP13) of 4-input NAND gate U5b presents a low to indicate that a sync cycle is detected. During TP13 is low, the output of U8c NAND gate is high, therefore the demodulator output is inhibited. For other output sets of Q0-Q3, TP13 presents a high.

The digital data on TP5 is also sent to the DATA input of the shift register U7. The clock frequency of U7 and U6b is 4fc, while bit rate of digital input data is equal to fc or 2fc. The frequencies of the counter (U6b) outputs Q1 and Q2 are fc and fc/2, respectively. The Q1 output is connected to the load input of the register U9 and to the RX CLK OUT terminal. The counter is reset either a sync cycle detected (TP13=0, CR=1) or Q2 output is high (Q2=1, CR=1).

The output of the demodulated data on U7 outputs Q2-Q3 is controlled by the control logic (NAND gates U8a, b, c, d). If no sync cycle is detected (TP13=1), the demodulated data can be sent to DATA OUT terminal. If a sync cycle is detected (TP13=0), the data path is blocked by the control logic.

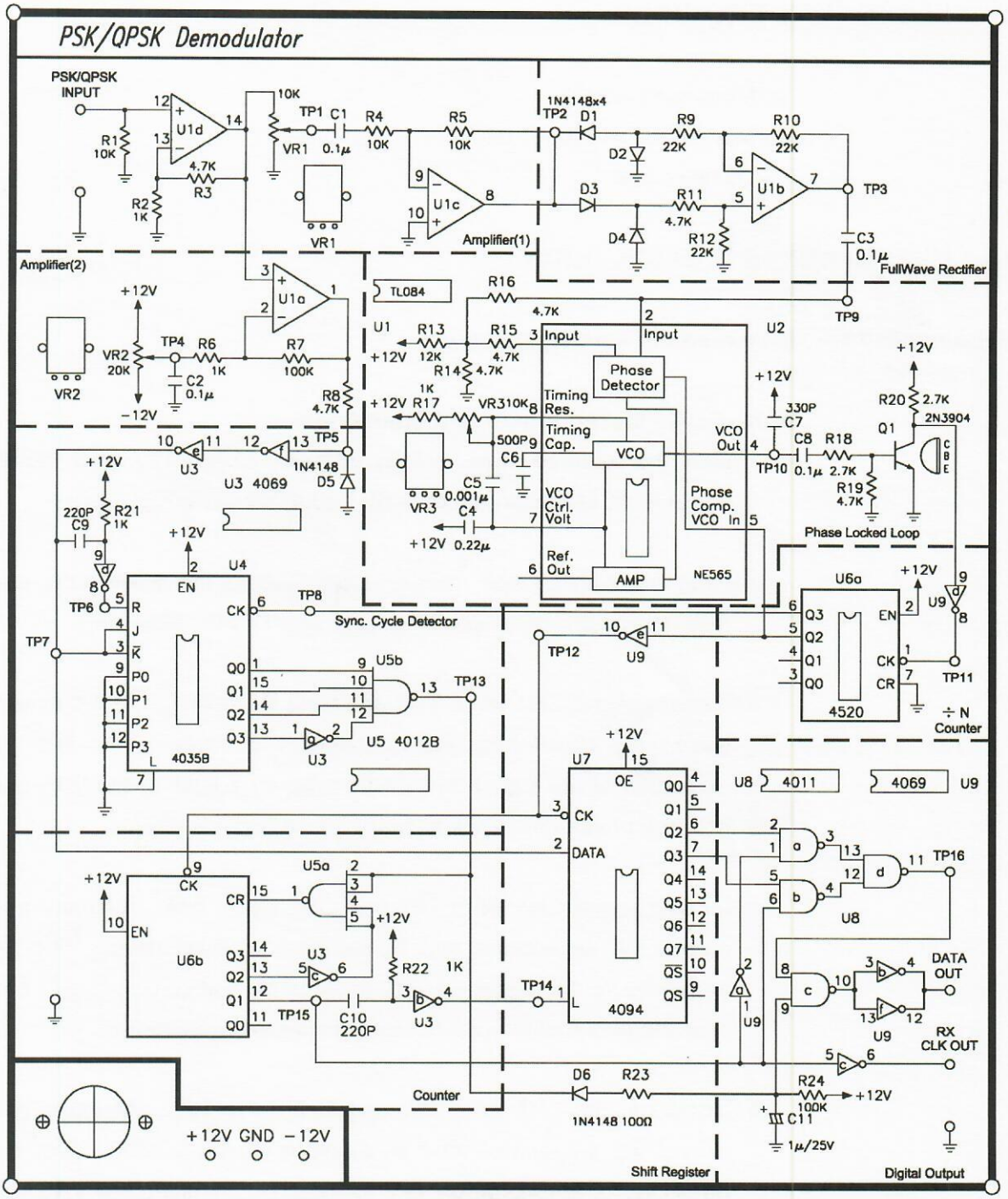

Figure 19-10 KL-94007 module

19.3 EQUIPMENT REQUIRED

1 - Module KL-96001
2 - Module KL-94006,KL-94007
3 - Oscilloscope

19.4 EXPERIMENTS AND RECORDS

Experiment 19-1 Measurement and Adjustment

A. KL-94006 Measurement and Adjustment

1.Apply the required power supply voltages +12V, -12V, and +5V to PSK/QPSK Modulator module KL-94006 shown in Figure 19-9.

2.Using the oscilloscope, measure and record the waveforms and frequencies on test points TP1, TP2, and TP3 in Table 19-2.

3.Connect scope CH1 IN to TP3 and CH2 IN to TP4. Measure and record the waveforms and frequencies in Table 19-3. Set the amplitude of the signal on TP4 to 1Vpp by adjusting the VR1 and note the phase difference between these two waveforms.

4.Connect scope CH1 IN to TP3 and CH2 IN to TP6. Measure and record the waveforms and frequencies in Table 19-3. Set the amplitude of the signal on TP6 to 2Vpp by adjusting the VR2 and note the phase difference between these two waveforms.

5.Connect scope CH1 IN to TP3 and CH2 IN to TP5. Measure and record the waveforms and frequencies in Table 19-3. Set the amplitude of the signal on TP5 to 3Vpp by adjusting the VR3 and note the phase difference between these two waveforms.

6.Connect scope CH1 IN to TP3 and CH2 IN to TP7. Measure and record the waveforms and frequencies in Table 19-3. Set the amplitude of the signal on TP7 to 3Vpp by adjusting the VR4 and note the phase difference between these two waveforms.

7. Connect a 500Hz, TTL-level square wave to the Digital DATA IN terminal.

8. Connect scope CH1 IN to the PSK/QPSK OUT. Measure the waveform and set the output amplitude to 10Vpp by adjusting the VR5 and record the result in Table 19-4. (Note: The frequency can not be measured in this case.)

9. Turn off the power.

10. Connect the PSK/QPSK OUT of module KL-94006 to the PSK/QPSK INPUT of module KL-94007.

11. Connect the power supply voltages required to both KL-94006 and KL-94007 modules.

B. KL-94007 Measurement and Adjustment

12. Connect scope CH1 IN to TP4. Measure and set the dc voltage to -5Vdc exactly by adjusting the VR2. To do this well, an extra DVM is a good choice.

13. Connect scope CH1 IN to TP1. Measure the waveform and frequency and set the amplitude to 5Vpp by adjusting the VR1. Record the result in Table 19-5.

14. Connect scope CH1 IN to TP11. Measure the waveform and frequency and set the frequency to 32fc by adjusting the VR3. Record the result in Table 19-6. If the carrier frequency is 8KHz, the signal frequency on TP11 should be 256KHz.

15. Connect scope CH1 IN to DATA OUT. Measure and record the waveform and frequency in Table 19-7. The waveform on DATA OUT should be the demodulated digital signal, 500Hz. If not, you can slightly turn the VR1 or turn off and then on the power.

16. Connect scope CH1 IN to RX CLK OUT terminal. Measure and record the waveform and frequency in Table 19-7. The waveform on RX CLK OUT should be recovered carrier signal. If not, you can slightly turn the VR1 or turn off and then on the power.

17. Turn off the power.

Experiment 19-2 PSK/QPSK Modulator

A. 2fc Measurement (KL-94006)

1. Connect a 500Hz, TTL-level digital signal to Digital DATA IN.

2. Connect scope CH1 IN to TP12 and CH2 IN to TP13. Measure and record the waveforms and frequencies in Table 19-8. Compare the phase difference between these two waveforms.

3. Connect scope CH1 IN to TP15. Measure and record the waveform and frequency in Table 19-8. The frequency should be twice the carrier frequency, 2fc.

B. Sync Cycle Measurement

4. Measure and record the waveforms and frequencies on the test points listed in Table 19-9.

C. Control Shift Register Measurement

5. Connect scope CH1 IN to TP10 and CH2 IN to TP11. Measure and record the waveforms and frequencies in Table 19-10.

6. Repeat step 5 for digital signal frequencies 100Hz and 1KHz to Digital DATA IN.

7. Recover the digital signal frequency to 500Hz.

D. PSK/QPSK modulated Signal Measurement

8. Connect scope CH1 IN to PSK/QPSK OUT. Measure and record the waveform with the various TIME/DIV settings in Table 19-11.

Experiment 19-3 PSK/QPSK Demodulator

A. Sync Cycle Detector Measurement (KL-94007 module)

1. Connect a 500Hz, TTL-level square wave to the **Digital DATA IN** terminal.

2. Set DC voltage on **TP4** to the values listed in Table 19-12. Using the scope, measure and record the waveforms and frequencies on **TP5**, **TP6**, **TP7**, and **TP13** for each dc setting value in Table 19-12.

3. Set DC voltage on **TP4** to -5V.

B. Full-wave Rectifier Measurement

4. Connect TTL-level square wave with the frequencies, listed in Table 19-13, to Digital DATA IN terminal. Using the scope, measure and record the waveforms and frequencies on TP2, TP3, and TP9 for each input frequency in Table 19-13.

5. Connect a 500Hz, TTL-level square wave to the Digital DATA IN terminal.

C. 32fc, 4fc and 2fc Measurement

6. Measure the frequency on TP11 to obtain a frequency equal to 32fc by adjusting the VR3. Measure and record the waveforms and frequencies on TP11, TP8, and TP12 in Table 19-14.

D. Shift Register Measurement

7. Measure and record the waveforms and frequencies on TP7, TP12, TP14, U7 Q2, and U7 Q3 in Table 19-15.

E. Demodulator Output Measurement

8. Measure and record the waveforms and frequencies on DATA OUT and RX CLK OUT in Table 19-16.

9. Repeat step 8 for the Digital DATA IN frequencies of 100Hz and 1KHz.

Table 19-2 Measurement and adjustment (KL-94006 module)

Test Point	Frequency	Waveform
TP1		
TP2		
TP3		

Table 19-3 Measurement and adjustment (KL-94006 module)

Test Point	Waveform & Frequency
TP3	
TP4	
TP5	
TP6	
TP7	

Table 19-4 Measurement and adjustment (KL-94006 module)

Test Point	Waveform
PSK/QPSK OUT	

Table 19-5 Measurement and adjustment (KL-94007 module)

Test Point	Waveform & Frequency
TP1	

Table 19-6 Measurement and adjustment (KL-94007 module)

Test Point	Waveform & Frequency
TP11	

Table 19-7 Measurement and adjustment (KL-94007 module)

Test Point	Waveform & Frequency
DATA OUT	
RX CLK OUT	

Table 19-8 2fc Measurement (KL-94006 module)

Test Point	Waveform & Frequency
TP12 (CH1) TP13 (CH2)	
TP15	

Table 19-9 Sync cycle measurement

Test Point	Waveform & Frequency
TP15	
TP16	
TP8	
TP17	

Table 19-10 Shift register measurement

Digital DATA IN Frequency	Test Point	
	CH1=TP10	CH2=TP11
500Hz		
100Hz		
1KHz		

Table 19-11 PSK/QPSK modulated signal measurement

Scope TIME/DIV	PSK/QPSK OUT
2.5ms	
1ms	
500μs	
250μs	
100μs	

Table 19-12 Sync cycle detector measurement (KL-94007 module)

TP4 DC voltage	Test Points			
	TP5	TP6	TP7	TP13
-5Vdc				
-3Vdc				
-1Vdc				
0Vdc				
+3Vdc				

Table 19-13 Full-wave rectifier measurement

Digital DATA IN Frequency (KL-94006)	Test Points		
	TP2	TP3	TP9
500Hz			
100Hz			
1KHz			

Table 19-14 32fc, 4fc and 2fc measurement

Test Point	Waveform & Frequency
TP11 (32fc)	
TP8 (2fc)	
TP12 (4fc)	

Table 19-15 Shift register measurement

Test Point	Waveform & Frequency
TP12	
TP7	
TP14	
U7 Q2	
U7 Q3	

Table 19-16 Demodulator output measurement

Digital DATA IN Frequency (KL-94006)	Test Point	
	DATA OUT	RX CLK OUT
500Hz		
100Hz		
1KHz		

19.5 QUESTIONS

1. Explain why the signal frequency on PSK/QPSK OUT terminal couldn't be measured in step 8 of experiment 19-1.

2. Explain why the demodulator output signal on DATA OUT terminal couldn't be stable on scope screen sometimes.