Chapter 16

CVSD SYSTEM

16.1 OBJECTIVES

1. To study the principle of DM system.
2. To study the principle of CVSD system.
3. To implement CVSD modulator and demodulator.

16.2 DISCUSSION OF FUNDAMENTALS

Delta modulation (DM) is a pulse coding technique which requires much simpler hardware than pulse-coded modulation (PCM) and involves sending the difference between each sample of the analog signal and the preceding sample, instead of sending the samples themselves.

Linear DM

Figures 16-1 and 16-2 show the functional block diagram and waveforms of a linear DM system, respectively. The operation of the DM system is described as follows.

1. The analog input signal is approximated by a signal composed of steps, which is produced by integration of Δ weighted impulses. If the analog input signal S(t) is greater than the approximation signal $\overline{S}(t)$, then the output of the comparator $\Delta(t)$ is +1 and the output of the multiplier Po(t) is a positive impulse, integrator integrates the positive impulse and $\overline{S}(t)$ is increased by Δ.

2. If $S(t)<\overline{S}(t)$, then the comparator output is low, then the output of the comparator $\Delta(t)$ is -1 and the output of the multiplier Po(t) is a negative impulse, integrator integrates the negative impulse and $\overline{S}(t)$ is decreased by Δ.

3. The multiplier output Po(t) is composed of positive and negative impulses. Positive impulse is shaped to a high and negative impulse is shaped to a low. Therefore the DM output signal $P\tau(t)$ is a binary data stream.

4. In demodulator, the received data stream $P\tau(t)$ is integrated by the integrator, which has the same characteristic as modulator's integrator. The integrator produces an analog output $\hat{S}(t)$ which is very like S(t) signal. The lowpass filter (LPF) removes the sawtooth component of $\hat{S}(t)$ and reconstructs the analog signal S(t).

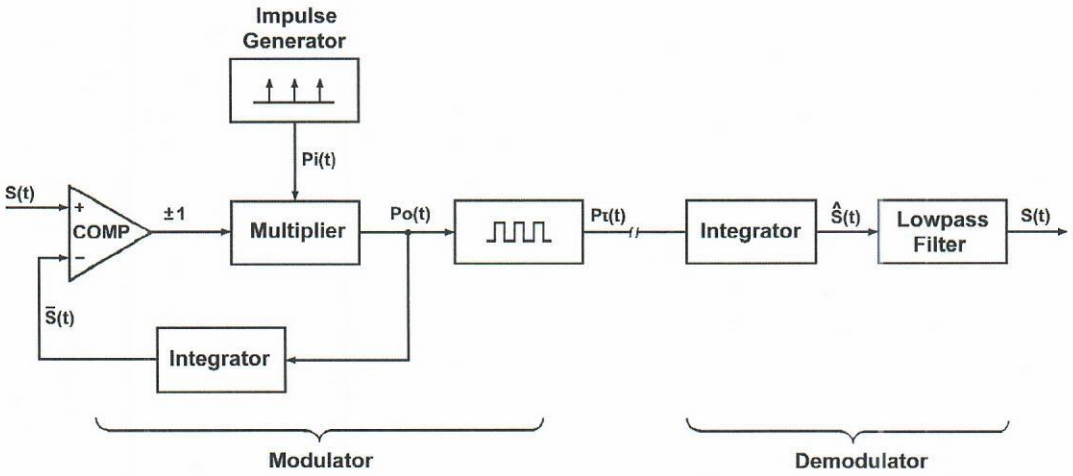

Figure 16-1 Block diagram of DM system

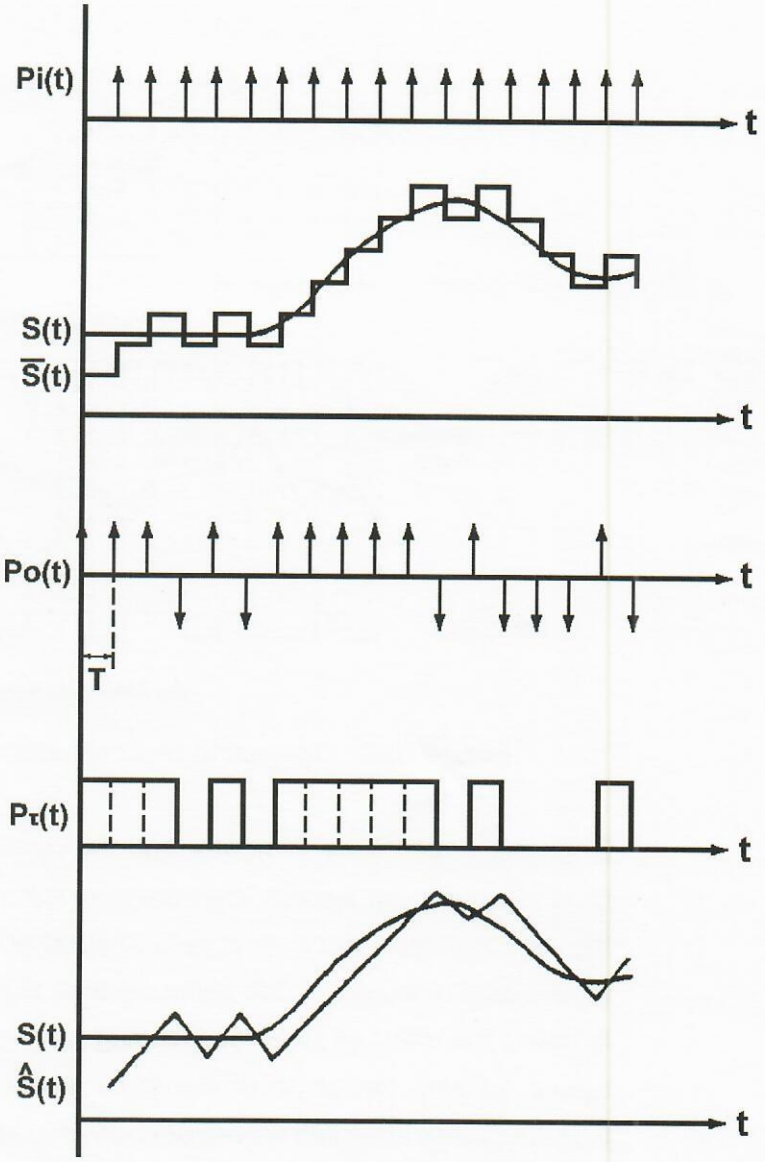

Figure 16-2 DM system waveforms

In practical DM systems the steps of the approximation signal are not formed by integrating impulses, since it is in practice impossible to produce impulses. Instead, the approximation signal is usually formed from triangular wave segments, which are produced by integrating pulses of finite duration. This is shown in Figure 16-3 where the pulse signal is generated by a pulse generator.

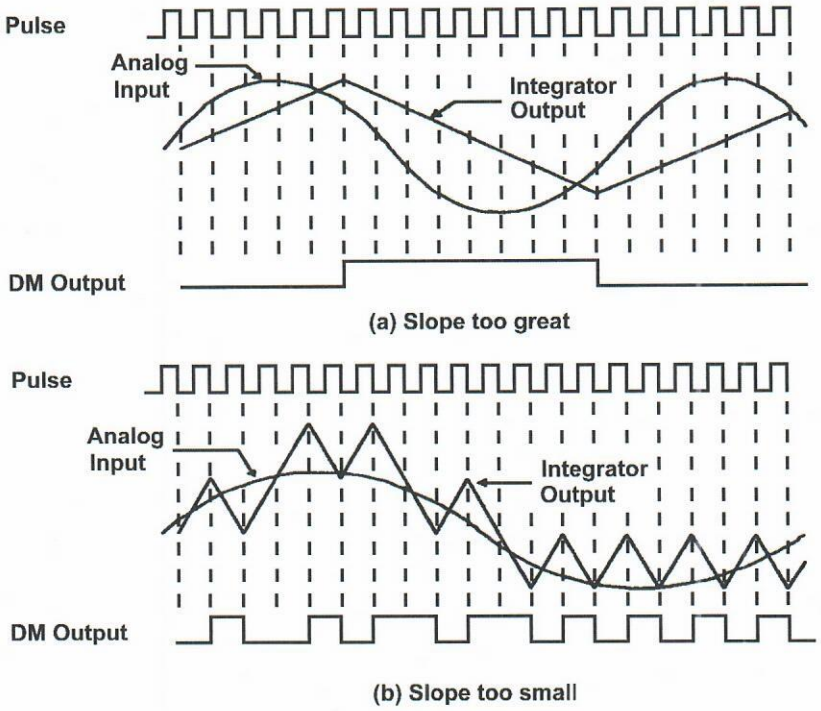

Figure 16-3 Integrating approximation and input signals

Since the slope of the integrator and the pulse train frequency are both fixed in a particular system, the maximum rate of increase or decrease of the approximation signal (integrator output) is fixed. If the slope of the input signal is too great, the approximation signal cannot follow it. This is called the effect of slope-overloading as shown in Figure 16-3(a). In Figure 16-3(b), the slope of the input signal is too small so that the high-frequency sawtooth waves are added to the approximation signal.

This disadvantage can be overcome by the use of continuously variable slope delta modulation (CVSD) system. Basically the slope of integrator in CVSD system is continuously increased and decreased to follow the slope of input signal.

CVSD System

The block diagram of CVSD system is shown in Figure 16-4. The operation of the CVSD system is interpreted as follows.

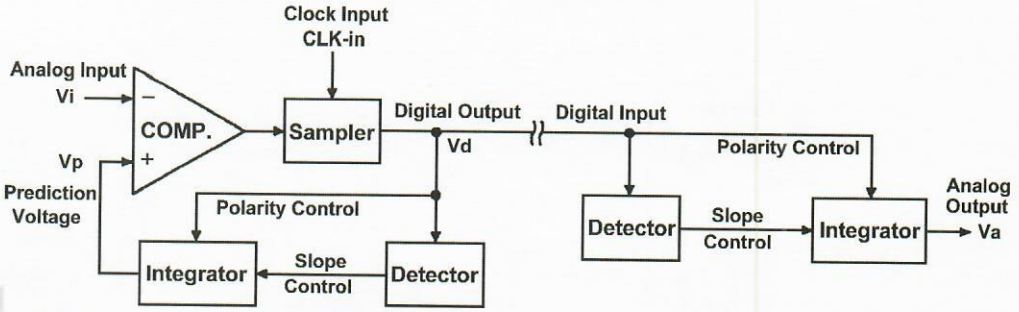

Figure 16-4 Block diagram of CVSD system

1. When the detector monitors n successive 0s or 1s on DM output, as the case of Figure 16-3(a), the slope of the integrator is identified too small and the slope is continuously increased to an appropriate value.

2. When the detector monitors n successive different data, as the case of Figure 16-3(b), the slope of the integrator is identified too great and the slope is continuously decreased to an appropriate value.

3. The number of n is specified to 3 in our experiments.

Practical Circuit Description

Figures 16-5 and 16-6 show the practical CVSD modulator and demodulator, respectively.

1. CVSD modulator
   (a) For CVSD modulation, the M/$\overline{I}$ input of U1 must be tied to 5V. A-in is analog input, D-out is the modulated digital output, U2 CLK-out is the clock pulse output. The clock frequency is adjustable in 50kHz to 100KHz range. Each sampling occurs on the negative-edge of clock pulse.
   (b) The dc component of analog input signal on A-in terminal is blocked by the coupling capacitor C1 and the peak-to-peak value of ac component must be not beyond 4V.
   (c) The modulated signal on D-out terminal is a TTL-level pulse train.

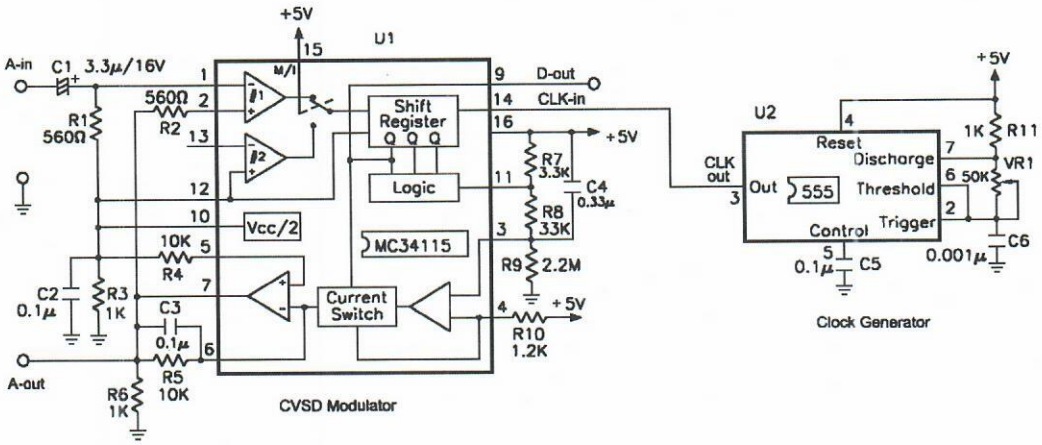

Figure 16-5 CVSD modulator

2. CVSD demodulator

(a) D-in terminal is the CVSD modulated signal input. DMA-out terminal is the reconstructed analog output. CLK-in terminal is the clock input.

(b) On the negative edge of clock pulse, the demodulator receives the CVSD modulated data and recovers the original analog signal.

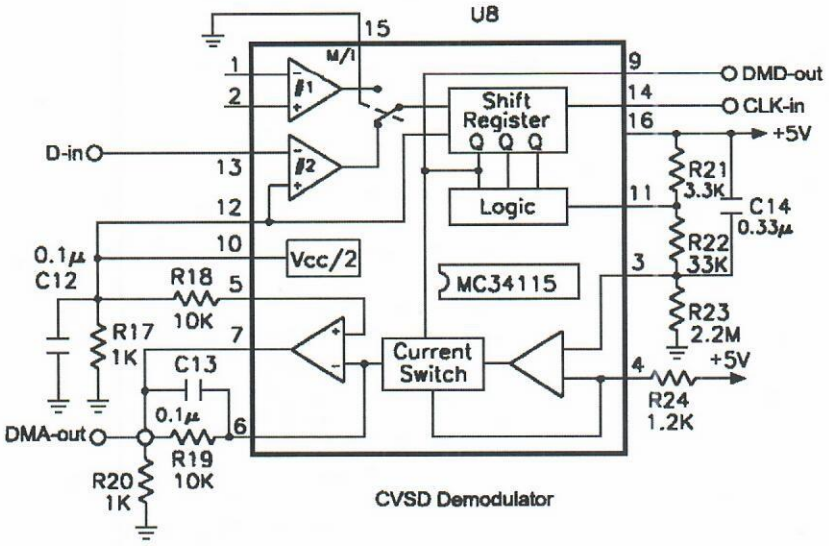

Figure 16-6 CVSD demodulator

Figure 16-7 shows the CVSD system containing the clock generator U2, the CVSD modulator U1, and the CVSD demodulator U8. U1 and U8 use the same chip MC34115. When the M/$\bar{I}$ pin is tied to 5V, the chip is used as a CVSD modulator. When the M/$\bar{I}$ pin is tied to 0V, the chip is used as a CVSD demodulator. The analog input signal is applied to the modulator input terminal, A-in, and the CVSD modulated data presents on the D-out terminal. The CVSD modulated data is directly connected to the input of demodulator (D-in) and the reconstructed analog signal presents at the output of the demodulator (DMA-out). In addition, the CVSD system uses the same clock signal so that the demodulator is synchronous with the modulator.

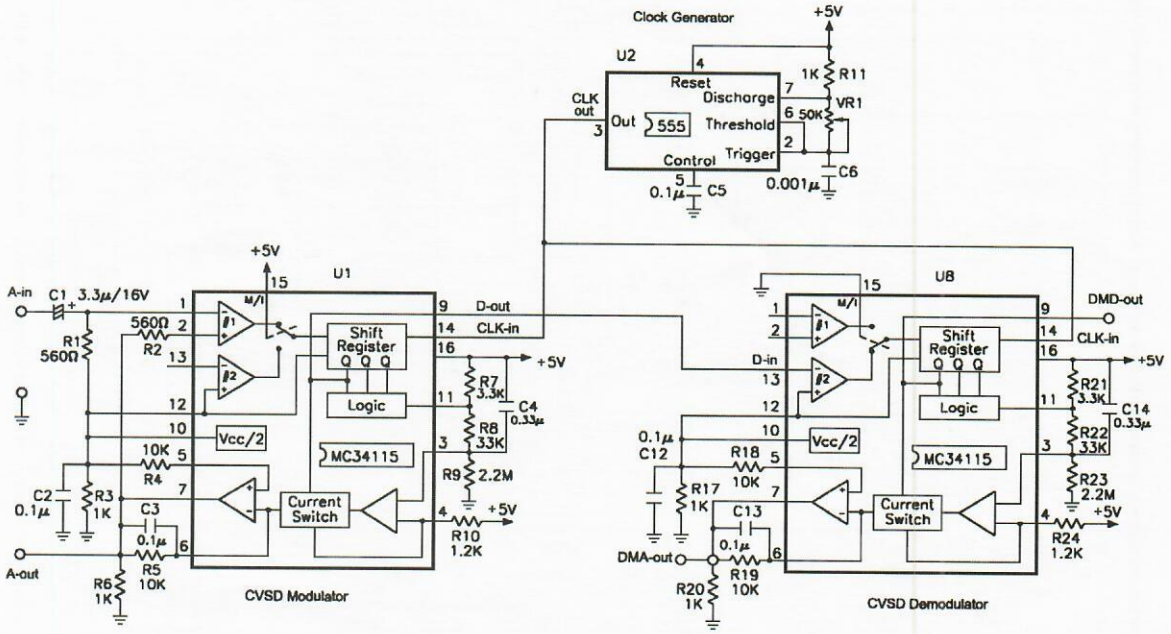

Figure 16-7 CVSD system

The entire circuits of CVSD modulator and demodulator are contained in KL-94004 Module shown in Figure 16-8.

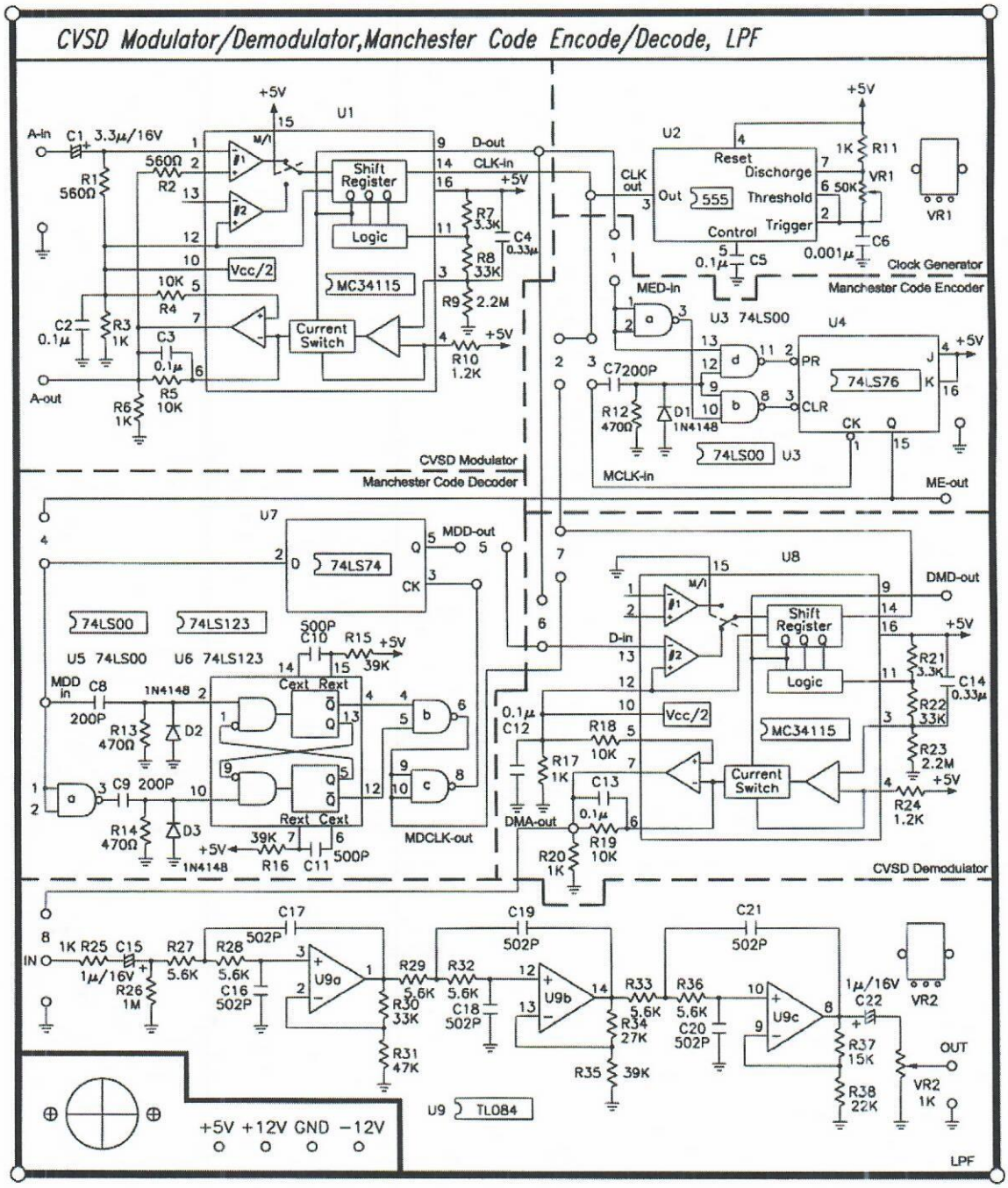

Figure 16-8 KL-94004 module

16.3 EQUIPMENT REQUIRED

1 - Module KL-96001
2 - Module KL-94004
3 - Oscilloscope

16.4 EXPERIMENTS AND RECORDS

Experiment 16-1 CVSD Modulator

1. Complete the CVSD modulator circuit of Figure 16-5 on KL-94004 module.

2. Connect scope input to CLK out terminal. Measure and read a clock frequency of 90KHz by turning the potentiometer VR1.

3. Connect a 1KHz, 1Vpp sinewave to A-in terminal. Measure and record the waveforms and frequencies on D-out and A-out terminals in Table 16-1. The signal on D-out terminal is a CVSD digital signal and the signal on A-out terminal is the approximation signal.

4. Using the storage oscilloscope, measure and hold the waveforms on A-out and D-out.
   During D-out at low, A-out signal is _____ (rising or falling).
   During D-out at high, A-out signal is _____ (rising or falling).

   Hold and view CLK out and D-out waveforms. The D-out signal is changed at the _____ (positive or negative) edge of clock pulse.

5. Connect a 3KHz, 1Vpp sinewave to A-in terminal and repeat step 3.

6. Connect a 200Hz, 1Vpp sinewave to A-in terminal and repeat step 3.

Experiment 16-2 CVSD Demodulator

1. Place jumpers in positions 2 and 6 to complete the CVSD demodulator shown in Figure 16-6.

2. Connect a 1KHz, 1Vpp sinewave to A-in terminal. Measure and record the waveforms on DMA-out and DMD-out terminals in Table 16-2.
   Compare DMA-out signal with A-in signal.
   Is the DMA-out signal identical to the A-in signal?
   _____

3. Connect a 3KHz, 1Vpp sinewave to A-in terminal and repeat step 2.
   Is the DMA-out signal more close to the A-in signal?
   _____
   Does the sawtooth component of DMA-out signal increase?
   _____

4. Connect a 200Hz, 1Vpp sinewave to A-in terminal and repeat step 2.
   Is the DMA-out signal more close to the A-in signal?
   _____
   Does the sawtooth component of DMA-out signal increase?
   _____

Experiment 16-3 Lowpass Filter

1. Place jumpers in positions 2, 6, and 8 to complete CVSD system circuit shown in Figure16-7.

2. Connect a 1KHz, 1Vpp sinewave to A-in terminal. Measure and record the waveforms and frequencies on DMD-out, DMA-out, and LPF OUT in Table 16-3. Turn potentiometer VR2 to obtain LPF OUT signal identical to A-in signal.

3. Connect a 3KHz, 1Vpp sinewave to A-in terminal and repeat step 2.

4. Connect a 200Hz, 1Vpp sinewave to A-in terminal and repeat step 2.

Experiment 16-4 CVSD System at Various Clock Rates

1. Complete CVSD system circuit by placing jumpers in positions 2, 6, and 8.

2. Connect a 1KHz, 1Vpp sinewave to A-in terminal. Set clock output frequency on CLK out to 90KHz by turning the potentiometer VR1. Measure and record the waveforms and frequencies on DMD-out, DMA-out, and LPF OUT in Table 16-4. Adjust potentiometer VR2 to obtain LPF OUT signal identical to A-in signal.

3. Set clock output frequency at CLK out to 50KHz and repeat step 2.

4. Set clock output frequency at CLK out to 70KHz and repeat step 2.

5. Set clock output frequency at CLK out to 100KHz and repeat step 2.

Table 16-1 CVSD modulator (CLK out = 90KHz)

A-in Input Signal	A-out Waveform & Frequency	D-out Waveform & Frequency
1KHz 1Vpp Sinewave		
3KHz 1Vpp Sinewave		
200Hz 1Vpp Sinewave		

Table 16-2 CVSD demodulator (CLK out = 90KHz)

A-in Input Signal	DMD-out Waveform & Frequency	DMA-out Waveform & Frequency
1KHz 1Vpp Sinewave		
3KHz 1Vpp Sinewave		
200Hz 1Vpp Sinewave		

Table 16-3 Lowpass filter (CLK out = 90KHz)

A-in Input Signal	DMD-out Waveform & Frequency	DMA-out Waveform & Frequency	LPF OUT Waveform & Frequency
1KHz 1Vpp Sinewave			
3KHz 1Vpp Sinewave			
200Hz 1Vpp Sinewave			

Table 16-4 CVSD system operating at different clock rates
(A-in = 1KHz, 1Vpp sinewave)

CLK out Frequency	DMD-out Waveform & Frequency	DMA-out Waveform & Frequency	LPF OUT Waveform & Frequency
50KHz			
70KHz			
90KHz			
100KHz			

16.5 QUESTIONS

1. Discuss the relationship between DMA-out and A-out signals.

2. Explain the results of steps 3 and 4 in Experiment 16-2.

3. Describe the function of the lowpass filter (LPF) used in CVSD system.